IPC/NETARM-1A

Document Ordercode: DOC/IPC_NETARM-E

Revision	Date	Author	Modification
1.0	27.11.2006	S. Wyss	Draft/Preliminary
1.1	08.12.2006	S. Wyss	Revision
1.2	22.01.2007	S. Wyss	Korrex
1.3	10.04.2007	S. Wyss	Korrex
1.4	12.12.2007	S. Wyss	PCB #4 Revision
1.5	09.01.2008	S. Wyss	IRQ Interrupts
1.6	29.04.2009	P. Brunner	Errata Table 6 and Table 8

Contents

List of Tables

List of Figures

1 Product Overview

1.1. Introduction

The IPC/NETARM is an industrial Single Board Computer from *Syslogic* based on the EP9315 processor from *Cirrus Logic*. It features an advanced 200MHz ARM920T (ARM9) processor core with high performance at low power consumption.

Although it is based on a different processor architecture, the IPC/NETARM is a drop-in replacement for the x86 based IPC/NETIPCs because it has the same PC/104 bus interface and also the same connector positions.

The Syslogic IPC/NETARM processor board is also very similar to the EDB9315A evaluation board from the processor supplier *Cirrus Logic*. Most of the binary operating system images from *Cirrus Logic* run without any modification on the IPC/NETARM.

1.2. Board Features

High-Performance ARM920T Processor Core

- low power industrial processor eliminating the need for enforced cooling.
- high performance 32-bit 5-stage pipeline ARM9 based processor core (ARM920T) with Thumb Instruction Set.
- 200 MHz processor clock speed
- 64 Mbyte SDRAM on board
- 16kByte data and 16kByte instruction caches

MaverickCrunch Coprocessor for Fast Math Processing

- single and double-precision integer and floating point processing.
- single cycle integer multiply and accumulate (MAC).

PC/104 Bus Interface

- PC/104 bus interface for expansion with standard 8/16 bit PC/104 communications and I/O boards.
- IRQ's supported.
- DMA supported.

USB 2.0 Full Speed Host

- up to 12 Mbps transfer rate
- 2 Ports, also Low Speed capable.

Graphics LCD & CRT Controller

- Digital Output: up to 1024x768 pixels (XGA) resolution, 24bit depth.
- Analog Output: standard analog RGB monitor interface.

Graphics Accelerator
- hardware graphics acceleration engine with block copy, block fill and hardware line draw operations.

Character LCD Interface
- standard 8bit character LCD interface, memory mapped to the system bus.

Serial Ports
- Two serial RS232 ports (COM1 with handshake, COM2 no handshake).
- COM2 can be assembled as a RS485 Port (half-duplex, no galvanic isolation).

Compact Flash and IDE Interface
- CompactFlash Type I connector for onboard mountable CompactFlash card configurable as master or slave IDE device (replacing one of the external IDE devices).
- standard 44 pin IDE connector (2mm pin raster) for two external IDE devices.

10/100baseT Ethernet interface
- on-chip auto negotiation, 10/100Mbit and Full/Half-Duplex.
- separate serial EEPROM containing MAC address.

AC '97 2.1 Compatible Audio Codec
- Stereo Line Input
- MIC Input
- Stereo Line Output
- Headphones Output

PS/2 Keyboard or Mouse Port
- emulated on SPI processor port.

4x4 Keypad Interface
- for low cost user input.

Touch Screen Interface
- support for 4-,5- and 8- wire touch screen panels.

Real Time Clock
- battery backed.

Hardware Watchdog
- configurable for 100 ms or 1.6 s timeout and Non-maskable Interrupt (NMI) or hardware reset activation.

Temperature Supervisor
- temperature supervisor for software controlled power management.

32 pin DIL Socket for SRAM, DiskOnChip, EEPROM

- socket for user installable Socket Memory supporting various types and sizes of 32 and 28 pin SRAM, Flash and EEPROM devices and supporting DiskOnChip 2000 and DiskOnChip Millennium products.
- battery backed

Firmware Flash Memory

- 128Mbit (16MByte) Flash for Bootloader, Operating System and File Systems. (Optional 32Mbit/4MByte available)
- supports easy firmware update through serial port

1.3. Board Block Diagram

Due to the high level of peripheral integration of the EP9315 processor, the NETARM board has a lot of peripheral connectors.

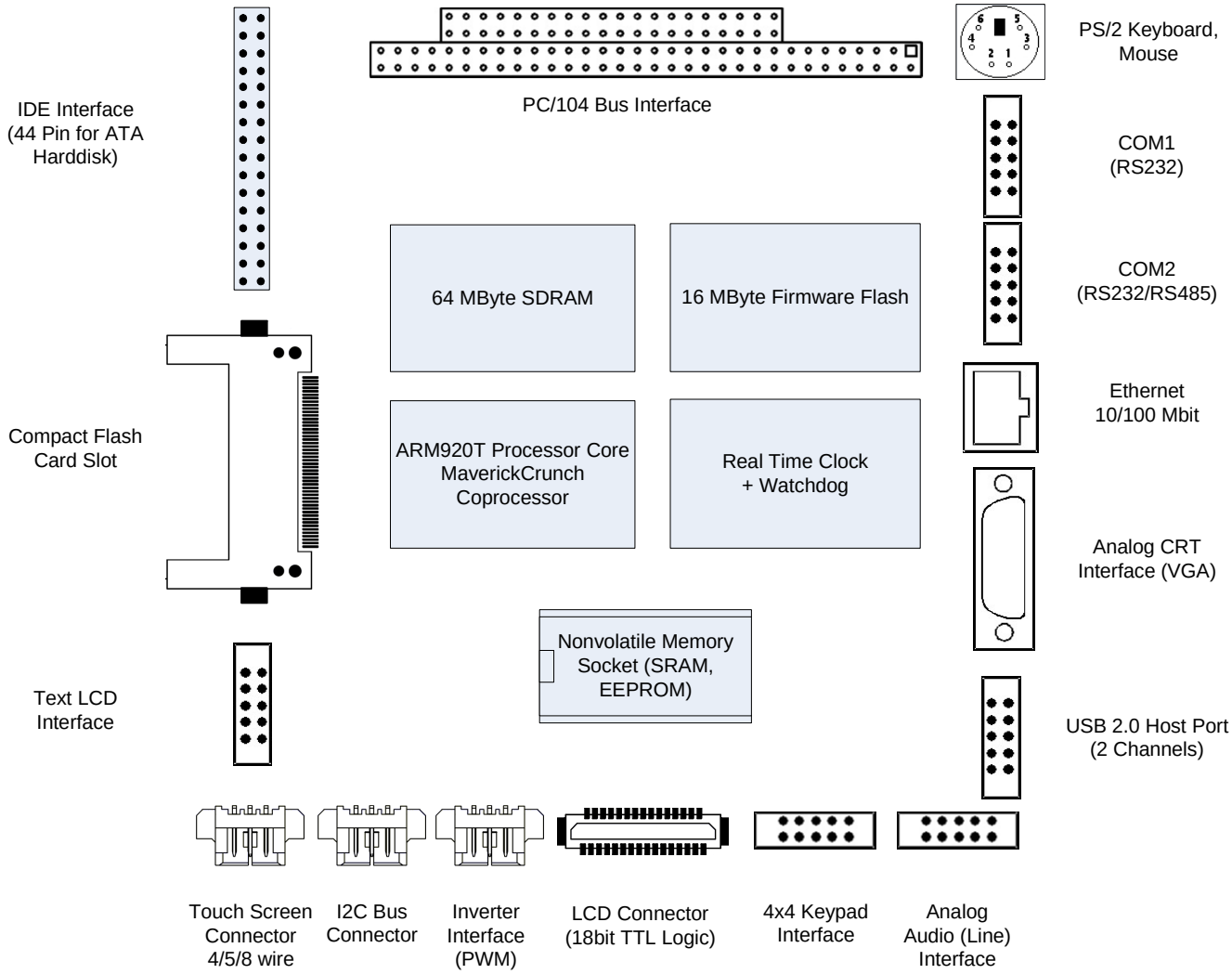

Figure 1 – Board Block Diagram

1.4. Startup Modes

The NETARM may startup either in “Normal” mode or in “Bootloader” mode. Bootloader mode is intended for updating the on-board firmware flash (not the Compact flash!).

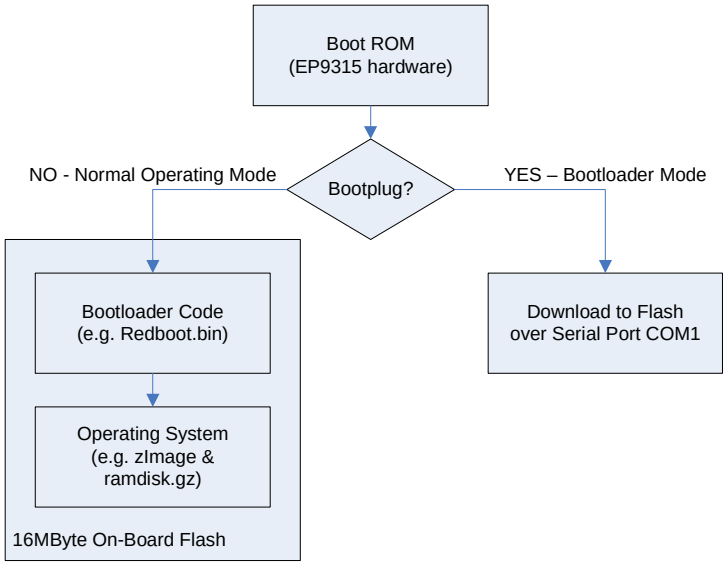

Figure 2 – Startup Modes

1.4.1. Bootloader Mode

Boot Loader mode is invoked when plugging a special Boot Loader Key (product code CUB/BOOTPLUG-1A) into the keyboard PS/2 connector (P3) or when setting switch S500-5 to ON state. In Boot Loader mode the content of the Onboard Flash may be updated over a serial port connection (COM1) from a Windows based host PC.

Figure 3 – Bootplug

Normal operating mode is invoked when no Bootplug is plugged into the keyboard connector.

Important Note

Please first-pull back the cover of the Bootplug when inserting the Bootplug into the PS/2 connector.

2 Board Description

2.1. Connector and Jumper Positions

The NETARM board hardware can be configured by jumpers. The jumper and connector locations are shown in the board layout drawing (Figure 4 - Board Layout).

Important Note

Always check the jumper configuration of a freshly received board to comply with your system requirements before applying power, otherwise the system may get damaged or may fail to operate.

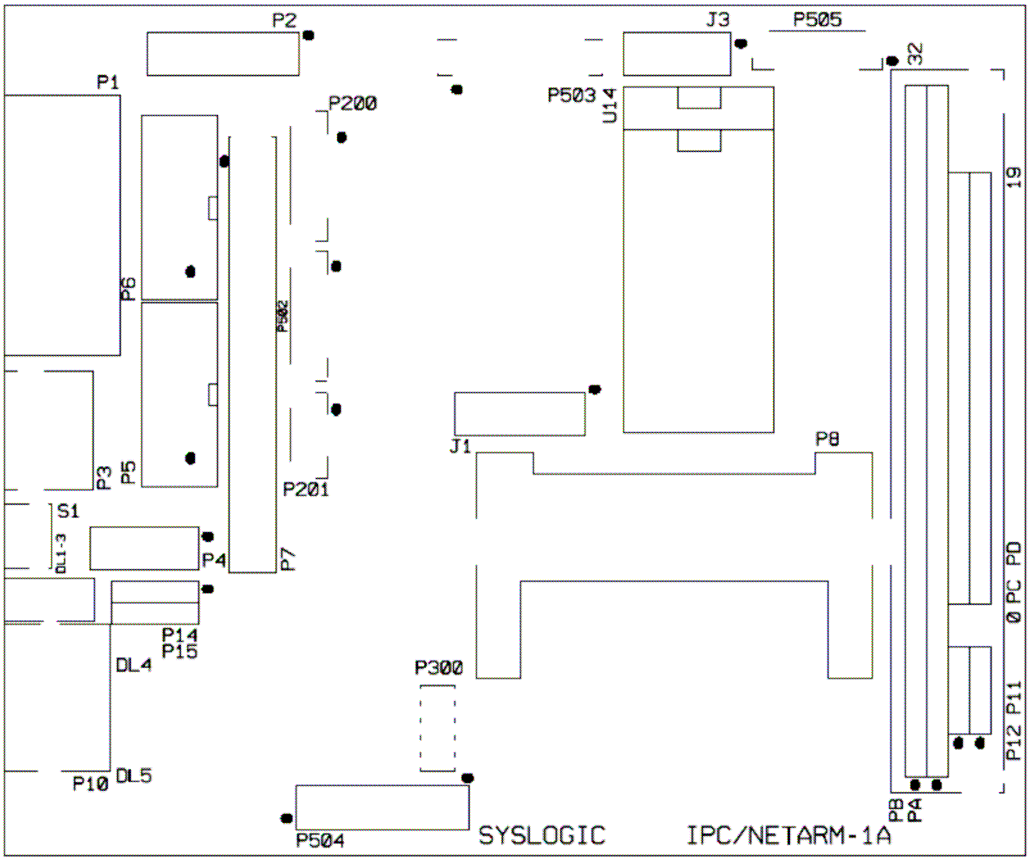

Figure 4 - Board Layout

2.2. EP9315 Processor Details

The Cirrus EP9315 system-on-chip processor has a built in 32bit ARM920T core with a memory management unit and 16kB instruction cache and 16kB data cache. The processor can also work in 16Bit mode (ARM Thumb Instruction Set) to provide higher code density and lower program space requirements.

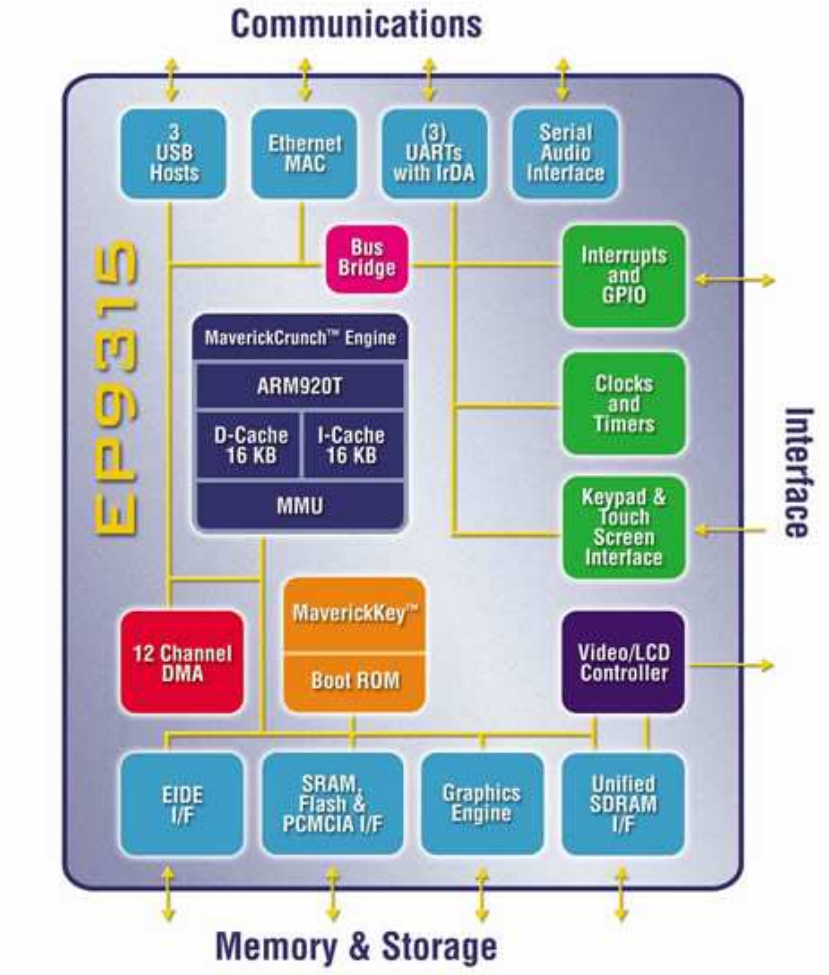

Figure 5 – CPU Block Diagram

The MaverickCrunch is a DSP engine that enhances the ARM920T core with fast floating point arithmetics.

3 Board Initialization Sequence

3.1. General

The IPC/NETARM does not provide a system BIOS (Basic Input Output System) like the x86 architecture based boards do. It is the booloader or the operating system's task to initialize the hardware peripherals.

Important Note

Some bootloaders or OS's available from Syslogic might have already implemented the initialisation sequences. But if you plan to use your own boot code or bootloader, you must assert that your code executes the necessary initialization before using the peripherals.

The following instructions only detail the initialization requirements for the external peripherals added by Syslogic. For initialization requirements of the internal CPU peripherals, please consult the EP9315 User's Guide [1].

3.2. Setup Memory Timing

Each different memory bank has its own bus access timing requirement and thus it is important to set up the static memory controller (SMC) for proper timings (i.e. wait states) before accessing that bank. Each memory bank can be programmed individually through its SMC configuration register. Please see the EP9315 User's Guide [1] page 489 for the register layout of the SMC configuration register.

The wait state generator of the SMC is clocked from the system's FCLK and therefore all wait state settings of the SMC registers rely on the chosen FCLK frequency. The following table details the recommended SMC configuration register values that need to be programmed to access each memory bank, given a maximum allowed system FCLK of 200 MHz.

Important Note

All software images downloadable from CIRRUS (e.g. Embedded Linux, Windows CE or ECOS) are configured for FCLK=200 MHz and thus only run on the IPC/NETARM-1A.

IPC/NETARM-1AE (industrial grade) has a maximum allowed FCLK of 184 MHz, so you need to reconfigure that clock setting in software, i.e. you are not allowed to run the binary images provided from CIRRUS directly on the IPC/NETARM-1AE.

3.2.1. Memory Banks with adjustable Wait States

The following table details the memory banks 0, 1 and 6 with adjustable wait states. You must program the "Required Values" into the SMC register before using each of the following memory banks.

Register Name	Setup Register Address	Required Value	Size	RD*/ WR*	Remarks
SMCBCR0 SMCBCR6 **FLASH**	0x8008'0000	0x1C00'1DC1	16bit	150ns(1) 160ns(2)	Bursts allowed
SMCBCR1 **SRAM**	0x8008'0004	0x0000'05C1	8bit	150ns(1) 160ns(2)	Burst not allowed

(1) IPC/NETARM-1A (commercial temp.) with 200MHz system clock.
(2) IPC/NETARM-1AE (industrial temp.) with 184MHz system clock.

Table 1 – Mem. Banks with Adjustable Wait States

3.2.2. Memory Banks with fixed Wait States

Memory Bank 2, 3 and 7 have an external WAIT STATE generator that is hard coded into the glue logic of the NETARM board. Thus the WAIT STATES of these memory bank does not correspond to the settings of the corresponding SMCBCRx register and can not be adjusted. Nevertheless, the SMCBCRx registers must be programmed with the following required register values (i.e. the memory access length bits must be programmed to 8 or 16 bits).

Register Name	Setup Register Address	Required Value	Size	RD*/ WR*	Remarks
SMCBCR2 **PC/104 8bit**	0x8008'0008	0x0000'FD21	8bit	590ns	Bursts not allowed
SMCBCR3 **PC/104 16bit**	0x8008'000C	0x1000'FD21	16bit	315ns	Bursts not allowed
SMCBCR3 **Character LCD 8bit**	0x8008'001C	0x0000'FD21	8bit	1000ns	Bursts not allowed

Table 2 – Mem. Banks with fixed Wait States

3.3. Disable DMA Acknowledge

The DMA signal lines of the NETARM are multiplexed with the general purpose port E (GPIOE). As a default after power-up, the GPIOE function is selected and the pins are set to input with a high/active signal state. This sets the DMA acknowledge signal on the PC/104 bus active and the non-DMA PC/104 bus slaves do not respond to bus accesses.

So we must deactivate the DMA acknowledge signal before doing non-DMA PC/104 bus accesses. The following registers have to be written for disabling the DMA acknowledge.

Register Name	Setup Register Address	Requirement	Remarks
PBDDR	0x8084'0014	Bit 0 = 1	Enable output on EGPIO8
PBDR	0x8084'0004	Bit 0 = 0	Disable DMA Acknowledge

Table 3 – Disable DMA acknowledge

3.4. Setup STOP and READY LED status

The STOP and READY LEDs are also routed to the PC/104 bus connector and might influence the behavior of some expansion boards. So it is mandatory to set them to a well defined state.

Register Name	Setup Register Address	Requirement	Remarks
Control Register	0x2000'8201	Bit 4 = 1	Disable STOP* (red LED disabled)
Setup Register	0x2000'8205	Bit 7 = 1	Enable READY (green LED enabled)

Table 4 – Setup of Stop and Ready signals

Important Note

These registers must be accessed **after** the memory timings are set up.

3.5. Pseudocode for Initialization

The following code shows a possible initialization sequence for the peripherals discussed in the previous sections.

C-Style Pseudocode for System Initialization

```
unsigned char bval;
unsigned long lval;

/* PROTOTYPE FUNCTIONS */
mem_long_write(unsigned long address, unsigned long data);
mem_long_read(unsigned long address, unsigned long *data);
mem_byte_write(unsigned long address, unsigned char data);
mem_byte_read(unsigned long address, unsigned char *data);

/* SETUP PC/104 MEMORY TIMINGS */
mem_long_write(0x80080008,0x0000FD21);
mem_long_write(0x8008000C,0x1000FD21);

/* SETUP FLASH MEMORY TIMINGS */
mem_long_write(0x8008'0000,0x1C00'1DC1);

/* SETUP SRAM MEMORY TIMINGS*/
mem_long_write(0x8008'0004,0x0000'05C1);

/* SETUP TEXT LCD MEMORY TIMINGS */
mem_long_write(0x8008'001C,0x0000'FD21);

/* DISABLE DMA-ACK -> set ISA_AEN low */
mem_long_read(0x80840014,&lval);
mem_long_write(0x80840014,lval|0x01);
mem_long_read(0x80840004,&lval);
mem_long_write(0x80840004,lval&(~0x01));

/* CLEAR STOP BIT (CLEAR RED LED) */
mem_byte_read(0x20008201,&bval);
mem_byte_write(0x20008201,bval&~0x10);

/* SET READY BIT (SET GREEN LED) */
mem_byte_read(0x20008205,&bval);
mem_byte_write(0x20008205,bval|0x80);
```

Table 5 – Pseudocode for System Initialization

4 Memory Resources

4.1. Overview

The NETARM has one unified memory space (UMA) for all different peripherals and memory types. This memory space has 32 address lines with a total of 4 GigaBytes addressable. Note that the most significant address bits are decoded into chip select signals and are referred to as CSx (i.e. CS2 stands for address range 0x2000'0000 to 0x2FFF'FFFF).

Unlike the x86 architecture that has two different memory access modes (I/O or Memory access), the ARM has just one single address space where all system resources are mapped into.

4.2. Memory Map

The "Static Memory Controller" of the EP9315 processor controls the memory timings and can be set up differently for each CSx memory bank. This setup has been done for the operating systems that are supported by Syslogic. So the following information will mainly be of use for porting a new operating system to the IPC/NETARM cpu board. In general, see chapter 12 (page 479ff) of the EP9315 Users Guide [1] for programming information concerning the static memory controller.

The IPC/NETARM has the following memory map.

Physical Address		Device / Register	Remarks
0x0000'0000..	0x00FF'FFFF	FLASH Memory	16 MByte
0x1000'0000..	0x1007'FFFF	SRAM Socket Memory	Max. 512kByte
0x2000'0000..	0x2FFF'FFFF	PC/104 8bit IO & Memory	See 4.5.2
0x3000'0000..	0x3FFF'FFFF	PC/104 16bit IO & Memory	See 4.5.2
0x6000'0000..	0x60FF'FFFF	FLASH Memory	16 MByte (mirrored CS0)
0x7000'0000..	0x7000'0001	LCD Interface (8bit character LCD)	See 5.1
0x8000'0000..	0x8FFF'FFFF	CPU Configuration Registers	See [1]
0xC000'0000..	0xC3FF'FFFF	SDRAM	64Mbytes
All other addresses		Reserved	

Table 6 - Physical Memory Layout

4.3. Flash Memory

The NETARM firmware flash is 16MBytes in size and is mapped to memory bank CS0 and CS6 (mirrored). It is accessed with 16bit (HALF WORD) data bus operations.

4.4. SRAM Socket Memory

The NETARM features a DIL32 socket for user insertable memory devices like SRAM, NVRAM, EEPROM, Flash and DiskOnChip products. Supported devices and corresponding configuration is listed in the table below, maximum access time allowed is 150 ns for all devices. The SRAM can be backed-up with by battery for nonvolatile SRAM configuration.

Important Note

Do not insert devices not listed. This could damage the hardware.

Important Note

When inserting a 28 pin device into the 32 pin socket, pin 1 of the 28 pin device must be positioned at pin 3 of the DIL32 socket, otherwise the hardware may get damaged.

Memory Type	Manufacturer and Order Code	J1 Setting (pins 8,9,10,12 only)	J3 Setting
SRAM	**Static RAM (5V)**	**5V, Battery Backup enabled**	
128k x 8	Samsung: K6X1008C2D-DB70 Hitachi: HM628128BLP-7 STMicro: M68AF127BL70B6	8-10	1-3, 2-4, 5-6, 8-10
512k x 8	Samsung: K6T4008C1C-DB70 Hitachi: HM628512BLP-7 Mitsubishi: M5M5408AP-70L	8-10	1-3, 2-4, 5-6, 7-8
NVRAM	**Nonvolatile RAM (5V)**	**5V, Battery Backup disabled**	
32k x 8	ZMD: U637256DC70	9-10	1-3, 2-4, 5-6, 8-10
32k x 8	Simtek: STK16C88-W45	9-10	1-3, 2-4, 5-6, 8-10
NVRAM	**Nonvolatile RAM (3.3V)**	**3.3V, Battery Backup disabled**	
128k x 8	Simtek: STK16CA8-W45	10-12	1-3, 2-4, 5-6, 8-10
EEPROM	**EEPROM (5V)**	**5V, Battery Backup disabled**	
32k x 8	Atmel: AT28C256(E)-15PC Catalyst: CAT28C256(H)P-15 Hitachi: HN58C256AP-10 Xicor: X28C256P-15	9-10	1-3, 2-4, 5-6, 8-10
64k x 8	Catalyst: CAT28C512(H)P-15 SST: SST29EE512A-90-4C-PH Xicor: X28C512P-15	9-10	1-2, 3-5, 4-6, 8-10
128k x 8	Atmel: AT28C010(E)-15PC SST: SST29EE010A-120-4C-PH Xicor: X28C010D-15	9-10	1-2, 3-5, 4-6, 8-10
Flash	**Flash Memory (5V)**	**5V, Battery Backup disabled**	
128k x 8	AMD: Am29F010B-90PC Atmel: AT29C010A-15PC SST: SST39SF010-90-4C-PH	9-10	1-2, 3-5, 4-6, 8-10
512k x 8	AMD: Am29F040B-90PC Atmel: AT29C040A-15PC SST: SST39SF040-90-4C-PH	9-10	1-2, 3-5, 4-6, 7-8
Flash	**Note: PLCC32 to DIL32 socket converter required**	**5V, Battery Backup disabled**	
512k x 8	Fujitsu: MBM29F040C-90PD ST: M29F040-90K1	9-10	1-2, 3-5, 4-6, 7-8
DOC	**DiskOnChip (5V)**	**5V, Battery Backup disabled**	
DiskOnChip 2000	M-Systems: MD2200-Dxx	9-10	1-2, 3-5, 4-6, 8-10
DiskOnChip Millennium	M-Systems: MD2800-Dxx	9-10	1-2, 3-5, 4-6, 8-10

Table 7 – Socket Memory Configuration

4.5. PC/104 Bus Interface

4.5.1. General

The PC/104 bus interface of the NETARM allows expansion with a wide range of I/O and communications boards.

The electrical specification for the PC/104 expansion bus is identical to the x86 PC ISA bus. The mechanical specification allows for the very compact implementation of the ISA bus. The bus interface is described in the IEEE 996 and 996.1 standards documentation.

Basically, the PC/104 bus allows multiple peripheral boards in a 3.6 inch by 3.8 inch form factor to be added in a self-stacking bus. Since the electrical specification is identical (except for drive levels) to a standard PC ISA bus, standard peripherals such as COM ports, Digital I/O, Ethernet ports, and LCD drivers may be added easily.

4.5.2. PC/104 Memory Map

The x86 architecture has different bus timings for its ISA (I/O or Memory) bus accesses, and it has also different timings for 8 or 16 bit data transfers. So, PC/104 peripherals can be accessed in the NETARM physical address space in one of four address ranges depending upon whether they are emulating an x86 Memory or I/O cycle and whether it needs to be a 8-bit or a 16-bit data access.

Type	Physical Address		Device / Register	Remarks
8Bit I/O	0x2000'0000..	0x2000'7FFF	PC/104	32 KBytes
	0x2000'8000..	*0x2000'801F*	*Reserved*	
	0x2000'8200..	0x2000'820F	Board System Registers (no PC/104)	16 Bytes
	0x2000'8210..	*0x2000'821F*	*Reserved*	
	0x2000'8220..	0x2000'82FF	PC/104	256 Bytes
	0x2000'8300..	*0x2000'9FFF*	*Reserved*	
	0x2000'A000..	0x2000'FFFF	PC/104	24 KBytes
8Bit MEM	0x2200'0000..	0x22FF'FFFF	PC/104	16 MBytes
16Bit I/O	0x3000'0000..	0x3000'7FFF	PC/104	32 KBytes
	0x3000'8000..	*0x3000'9FFF*	*Reserved*	
	0x3000'A000..	0x3000'FFFF	PC/104	24 KBytes
16Bit MEM	0x3200'0000..	0x32FF'FFFF	PC/104	16 MBytes

Table 8 – PC/104 address space

I/O cycles on the PC/104 expansion bus strobe either IOR# or IOW#, while Memory cycles strobe the (S)MEMR# or (S)MEMW# signals.

For example, an IPC/DIO32 peripheral board (8bit I/O PC/104 module) can be jumper-selected to the base address 0x200, which would correspond to a x86 PC I/O base address of 0x200. Since this is an 8-bit peripheral, this device must be accessed on the NETARM at the physical base address of 0x2000'0200.

The NETARM board is not fully IEEE 996.1 (PC/104) compliant. The following restrictions and differences to the IEEE 996.1 specification apply:

- connector and mounting holes are compatible but the board dimensions are bigger (100 x 120 mm^2)
- The ENDXFER* signal is not monitored on the NETARM board which results in standard transfer cycle for the requested 'zero waitstate' cycle.
- IRQ3, IRQ4 and IRQ14 are not supported
- Only DMA Channel 2 (DREQ2 & DACK2) is supported. All other DMA channels are not supported.

The bus connector pinout is shown in Table 44 **– PC/104 Bus Connectors PA/PB, PC/PD**. For single board applications only the power pins should be connected. See paragraph 6.1 for electrical specification.

4.5.3. PC/104 IRQ interrupts

The IRQ interrupt inputs from the PC/104 bus slaves are connected to the EP9315 general purpose port F (GPIO F, alternate function PCMCIA). The signal mapping for these interrupts is the following:

PC/104 IRQ	EP9315 Pin	VIC Int. Nr.	Port F Bitmask
IRQ5	Port F[Bit 0]/WP	19	0x01
IRQ6	Port F[Bit 1]/MCCD1	20	0x02
IRQ7	Port F[Bit 2]/MCCD2	21	0x04
IRQ9	Port F[Bit 3]/MCBVD1	22	0x08
IRQ10	Port F[Bit 4]/MCBVD2	47	0x10
IRQ11	Port F[Bit 5]/VS1	48	0x20
IRQ12	Port F[Bit 7]/VS2	50	0x80
IRQ15	Port F[Bit 6]/READY	49	0x40

Table 9 – PC/104 IRQ pins

The interrupt properties of GPIO port F pins are individually configurable. Please see the EP9315 User's Guide ([1] chapter 28) for details on the interrupt configuration register.

4.6. Board System Registers

The Board System Registers are mapped into the 8bit I/O address window of the PC/104 bus. These registers must not be confused with the internal ARM CPU System Registers that configure the ARM CPU and its internal peripherals.

The Board System Registers can be used to access/configure various peripherals that are not integrated into the EP9315 processor chip.

Address	Device / Register	Remarks
0x2000'8200	Status Register	
0x2000'8201	Control Register	
0x2000'8202	Function ID Register	=0x59
0x2000'8203	Reserved	
0x2000'8204	Option ID Register	=0x84
0x2000'8205	Setup Register	
0x2000'8206	Revision ID Register	
0x2000'8207	Reserved	
0x2000'8208	Reserved	
0x2000'8209	Reserved	
0x2000'820A	Boot Mode Input Register	
0x2000'820B	I2C Register	
0x2000'820C .. 0x2000'820F	Reserved	do not access

Table 10 – Board System Registers

Status Register

Reading I/O Register 0x2000_8200:

D7	D6	D5	D4	D3	D2	D1	D0
OVERTMP*	LOBAT*	1	WDG*	1	1	ERRINT*	1

Description:

- ERRINT*: Error Interrupt Status
  0 = Error Interrupt pending on this module
  1 = no Error Interrupt pending on this module
  (state of PC/104 bus signal ISA_IOCHCK#)
- WDG*: Watchdog Status Flag (persistent after board reset)
  0 = Watchdog has timed out
  1 = Watchdog running or disabled
  Reset by issuing a hardware reset (see register 8204H)
- LOBAT*: Battery Status Flag
  0 = Battery voltage low
  1 = Battery voltage ok
- OVERTMP*: Temperatur Sensor Status Flag
  0 = programmed temperatur limit reached
  1 = temperatur ok (below limit)

Writing I/O Register 0x2000_8200:

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	reserved	Reserved	reserved	Reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Control Register

Reading I/O Register 0x2000_8201:

D7	D6	D5	D4	D3	D2	D1	D0
TRIGGER	WDTRIG	WDNMI	STOP*	TRIGSRC	1	0	1

Description:

- TRIGSRC: NETARM TRIGGER Signal Source Select
  0 = hardware timer (RTC clock, 32kHz)
  1 = software timer
- STOP*: NETARM STOP* Signal State
  0 = STOP* inactive (high)
  1 = STOP* active (low)
- WDNMI: Watchdog action Select
  0 = Watchdog timeout activates hardware reset
  1 = Watchdog timeout activates Non Maskable Interrupt
- WDTRIG: Watchdog Trigger
  any state change triggers the watchdog (timeout reset)
- TRIGGER: Direct Control for NETARM TRIGGER* Signal
  0 = TRIGGER* Signal low
  1 = TRIGGER* Signal high

Writing I/O Register 0x2000_8201:

D7	D6	D5	D4	D3	D2	D1	D0
TRIGGER	WDTRIG	WDNMI	STOP*	TRIGSRC	reserved	reserved	reserved

Description:

- TRIGSRC: NETARM TRIGGER* Signal Source Select
  0 = hardware timer
  1 = software timer
- STOP*: NETARM STOP* Signal State
  0 = STOP* inactive (high)
  1 = STOP* active (low)
- WDNMI: Watchdog action Select
  0 = Watchdog timeout activates hardware reset
  1 = Watchdog timeout activates Non Maskable Interrupt
- WDTRIG: Watchdog Trigger, state change triggers the watchdog
- TRIGGER: Direct Control for NETARM TRIGGER* Signal
  (if enabled by TRIGSRC bit in Control Register)
  0 = TRIGGER* Signal low
  1 = TRIGGER* high

TRIGSRC	TRIGGER* Source
0	Square Wave Output (32kHz) of Real Time Clock Device to TRIGGER* output
1	TRIGGER bit directly controls the TRIGGER* output

Table 11 – Trigger* Source Selection

Function ID Register

Reading I/O Register 0x2000_8202:

D7	D6	D5	D4	D3	D2	D1	D0
FID7	FID6	FID5	FID4	FID3	FID2	FID1	FID0

Description:

- FID7..0: Function ID
  0101'1001 (59H) = general NETARM board,
  subtype defined by Option ID Register

Writing I/O Register 0x2000_8202:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	Reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Option ID Register

Reading I/O Register 0x2000_8204:

D7	D6	D5	D4	D3	D2	D1	D0
OPT7	OPT6	OPT5	OPT4	OPT3	OPT2	OPT1	OPT0

Description:

- OPT7..0: Option ID
  1000'0100 (84H) = IPC/NETARM-1A version

Writing I/O Register 0x2000_8204:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X

Description:

- xxxxxxxx: Writing data A5H invokes a complete hardware reset (also clearing the Watchdog timeout status bit)

Setup Register

Reading I/O Register 0x2000_8205:

D7	D6	D5	D4	D3	D2	D1	D0
READY	WDEN	0	0	0	0	0	0

Description:

- WDEN: Watchdog Enable
  0 = Watchdog disabled
  1 = Watchdog enabled (running)
- READY: NETARM READY Signal State
  0 = READY inactive
  1 = READY active

Writing I/O Register 0x2000_8205:

D7	D6	D5	D4	D3	D2	D1	D0
READY	WDEN	reserved	reserved	Reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0
- WDEN: Watchdog Enable
  0 = Watchdog disabled (cannot be disabled while running)
  1 = enable Watchdog
- READY: NETARM READY Signal State
  0 = deactivate READY
  1 = activate READY

Revision ID Register

Reading I/O Register 0x2000_8206:

D7	D6	D5	D4	D3	D2	D1	D0
RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0

Description:

RID7..0:Revision ID
xxH=Logic Design revision ID (see Table 43 – Hardware Revision State

Important Note

This document always covers the latest product revision listed in **Table 42.**
Please contact the manufacturers technical support for upgrade options.

Writing I/O Register 0x2000_8206:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	Reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Boot Mode Input Register

Reading I/O Register 0x2000_820A:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	BM1	BM0

Description:

- BM1..0: Boot Mode Inputs
  0 = reserved (Factory Diagnostic Mode)
  1 = reserved
  2 = Boot Loader Mode
  3 = normal Operating Mode

Writing I/O Register 0x2000_820A:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	Reserved	reserved	Reserved	reserved	reserved	reserved

Description:

- reserved: reserved, do not write

I2C Register (for temperatur sensor control)

Reading I/O Register 0x2000_820B:

D7	D6	D5	D4	D3	D2	D1	D0
SCLO	SDAO	SCL	SDA	1	1	1	1

Description:

- SDA: Data Port Pin State
  0 = Pin State = Low
  1 = Pin State = High
- SCL: Clock Port Pin State
  0 = Pin State = Low
  1 = Pin State = High
- SDAO: Data Port Output Latch State
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)
- SCLO: Clock Port Output State
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)

Writing I/O Register 0x2000_820B:

D7	D6	D5	D4	D3	D2	D1	D0
SCLO	SDAO	X	X	X	X	X	X

Description:

- SDAO: Data Port Output Latch
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)
- SCLO: Clock Port Output
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)

5 Peripheral Connectors

5.1. General Remarks

The EP9315 system-on-chip processor assembled on the IPC/NETARM boards integrates most peripheral devices (e.g. graphics controller, serial ports, USB ports) that make up the system. Thus, the "EP9315 User's Guide [1] is a valuable source of information for programming the NETARM board peripherals. The following sections address mainly the external peripherals added by the board manufacturer and thus not described in the "EP9315 User's Guide".

5.2. Temperature Sensor

The Temperature Sensor is an LM75 compatible chip programmable through the I^2C board system register (see 4.5.3). This register hosts the I^2C data lines. The protocol of the I^2C bus specification must be programmed completely in software. Please ask the board manufacturer for sample code. For detailed programming information please refer to the National Semiconductor LM75 datasheet or similar documentation. Power on default setting for OVERTMP* signal mapped to the STATUS board register (see 0) is 80°C chip temperature.

5.3. Watchdog

The watchdog is disabled by default at poweron and must be enabled by the application program (WDGEN bit). If watchdog programming is done from application software level, before enabling the watchdog by setting the WDEN bit in the NETARM Setup Register, the watchdog action (RESET or NMI) must be programmed in the NETARM Control Register (bit WDNMI).

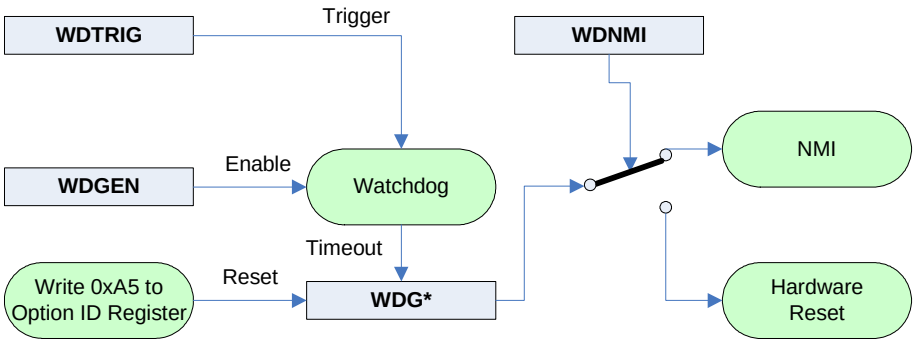

Figure 6 – Watchdog Block Diagram

If RESET activation is selected, the watchdog generates a hardware reset if it is not triggered within the configured timeout window by writing the WDTRIG bit in the NETARM Control Register. The application must check the WDG* bit in the NETARM Status Register upon startup to identify the Watchdog as the source of the reset, and it must issue a hardware reset (by writing the value 0a5h to the NETARM Option ID Register) to clear the WDG* flag. Otherwise the system resets again as soon as the Watchdog is started.

If NMI activation is selected, the watchdog generates a Non Maskable Interrupt to the processor if it is not triggered within the configured timeout window by writing the WDTRIG bit in the NETARM Control Register.

Important Note

The NMI interrupt is a feature from the x86 based processor world and has no direct match on ARM based processors. For reasons of board compatibility we still call this interrupt NMI on the NETARM board. The NMI is routed to **INT1** of the EP9315 processor, and INT1 must be set up correctly to handle the request.

The NMI is routed to the INT1 Pin of the EP9315 processor. You must set up the INT1 pin to handle the NMI Interrupt according to the EP9315 User's Guide [1].

The NMI routine must check the WDG* bit in the NETARM Status Register to identify the watchdog as the source of the NMI, and it must issue a hardware reset (by writing the value 0a5h to the NETARM Option ID Register) to clear the WDG* flag. Otherwise the NMI routine is entered again as soon as the watchdog is started.

Sample code showing the initialization and triggering of the watchdog is available from Syslogic.

5.4. 8-Bit Character LCD Interface

This Interface allows to connect a HD44780 (Hitachi Controller) based 8 Bit Character LCD to the NETARM without any external drive requirements. The following table details the connector layout:

Pin Number	Signal	Pin Number	Signal
1	GND	2	+5Vcc
3	CTR	4	RS
5	R/Wn	6	E
7	SD0	8	SD1
9	SD2	10	SD3
11	SD4	12	SD5
13	SD6	14	SD7
15	Vcc LED	16	GND

Table 12 – Char. LCD Connector P504 (Header 2.54mm)

The CTR (Contrast) Pin is driven by the PWM generator (PWMOUT, Pin U16) of the EP9315 processor that is averaged to a DC bias voltage with external circuitry. The NETARM is tested with at least the following character LCD's:

Manufacturer & Model	Type	Size
OPTREX C-51848NFQJ-LG-ACN	2x16 Chars, STN transm., GREEN	122x44mm

Table 13 – Tested Character LCD's

Please contact the manufacturer of the NETARM board for an up-to-date list of recommended and tested Character LCD displays and for sample code that implements the LCD programming. Display programming can be accomplished through the following register set that is available in the NETARM memory map.

Address	Device / Register	Remarks
0x7000'0000	Command Register	RS signal low
0x7000'0001	Data Register	RS signal high

Table 14 – Character LCD Registers

5.5. I²C Interface

The I²C Bus Interface is available on Connector P201. The clock (SCL) and data line (SDA) can be read or driven from the Board System Register "I2C Register" (see 4.5.3). Note that the LM75 system temperature sensor and the RTC (real time clock) are also connected on the I²C Bus.

The LM75 occupies the addresses 0x90h and 0x91h on the bus, the RTC reserves 0xD0h and 0xD1h.

Important Note

When using the I²C bus, always be aware of the fact that the I²C bus addresses 0x90h, 0x91h, 0xD0h and 0xD1h are reserved by the on-board temperature sensor and RTC.

Pin Number	Signal	Remarks
1	I²C DATA	(pulled-up 3.3V)
2	I²C CLOCK	(pulled-up 3.3V)
3	+3.3V (optional +5V available)	50mA max.
4	GND	

Table 15 – I²C Connector P201 (Molex)

5.6. VGA Interface

The VGA signals are available on the High Density DSUB15 connector P1 for direct connection of VGA compatible monitors. The signals are also available on the internal header P2 for special expansion boards that may convert the VGA signals into other display standards (e.g. PAL/NTSC or digital TFT).

Device Connection

Pin Number	Signal	Remarks
1	RED	
2	GREEN	
3	BLUE	
4	-	
5	GND	
6	GND	
7	GND	
8	GND	
9	+5V	not fused
10	GND	
11	-	
12	DDC Data	
13	HSYNC	
14	VSYNC	
15	DDC Clock	

Table 16 – VGA connector P1 (DSUB15HD)

Pin Number	Signal	Pin Number	Signal
1	RGB: TV_RED SVHS: C (Chrominance)	2	RGB: TV_GREEN SVHS: Y (Luminance)
3	RED	4	GREEN
5	BLUE	6	GND
7	Dot Clock	8	GND
9	HSYNC	10	VSYNC
11	DDC Data	12	DDC Clock
13	RGB: TV_BLUE	14	CVBS: Composite Video

Table 17 – VGA internal header P2 (2x7/2x5 pin)

Important Note

Be careful when using the VGA or video signals on expansion boards. Special design and layout precautions must be met for these high speed analog signals.
Maximum cable length allowed for VGA connection is 15 m.
Use high quality VGA cables (with coaxial wires for RGB signals) for maximum EMI protection.

Note

The NETARM-1A does not have Dot Clock and video outputs, therefore these signals are unconnected on the 2x7 pin header (pins 1,2,7,13,14).

5.7. TFT Data Interface

The TFT interface consists of a 31-pin header that allows to connect 18-bit colour TFT's with TTL signal levels. Also included is a TFT-Inverter connector with brightness control output and a configuration switch.

Pin Number	Signal	Pin Number	Signal
1	GND	2	CLK
3	HSYNC	4	VSYNC
5	GND	6	RED0
7	RED1	8	RED2
9	RED3	10	RED4
11	RED5	12	GND
13	GREEN0	14	GREEN1
15	GREEN2	16	GREEN3
17	GREEN4	18	GREEN5
19	GND	20	BLUE0
21	BLUE1	22	BLUE2
23	BLUE3	24	BLUE4
25	BLUE5	26	GND
27	BLANK	28	+3.3V
29	+3.3V	30	HMODE
31	VMODE		

Table 18 – TFT panel connector P503 (31 pin)

Pins 30 and 31 of the TFT connector P503 are connected to the inverter configuration switch S500 (pin 3 and pin 4) and might be used configure the TFT scan direction input.

5.8. TFT Inverter Interface

Switch Number	Signal	Remarks
1	SW1	
2	SW2	
3	HMODE	pull-up 3.3V
4	VMODE	pull-up 3.3V
5	BM0	pull-up 3.3V
6	Do not use	

Table 19 – TFT inverter configuration switch S500

SW1 and SW2 connect directly to the inverter connector P505 (pin7 and pin8) and may pull down these pins to ground if enabled. When the corresponding switches are set to off, these pins are floating.

BM0 is the boot mode selector switch. It can be used instead of a CUB/BOOTPLG bootloader key to set the IPC/NETARM in bootloader mode. If the switch is set to ON state, bootloader mode is enabled.

Pin Number	Signal	Remarks
1	+5V VCC	Inverter Power
2	+5V VCC	Inverter Power
3	GND	
4	GND	
5	LCD Enable (TTL)	Inverted EGPIO13
6	LCD Brightness (PWM 0..5V)	Brightness Control from raster engine
7	SW1	
8	SW2	

Table 20 – TFT inverter connector P505 (1x8)

Pin 5 (LCD enable) of the TFT inverter connetor is connected to the inverted EGPIO13 signal of the EP9315 processor. Pin 6 (LCD Brightness) is driven by the averaged PWM brightness control raster engine output (BRIGHT pin).

Note

The NETARM-1A can power an external inverter board for TFT CCFL applications. Maximum available current is 2.2 Amperes (at 5V).

5.9. TFT Touch Screen Interface

The EP9315 CPU supports 4-,5- and 8- wire resistive touch screens. The IPC/NETARM board brings these signals to the P502 connector:

Pin Number	Signal	Remarks
1	YP	Y-Axis positive
2	SYP	Sense Y-Axis positive
3	SYM	Sense Y-Axis negative
4	YM	Y-Axis negative
5	XM	X-Axis negative
6	SXM	Sense X-Axis negative
7	SXP	Sense X-Axis positive
8	XP	X-Axis positive

Table 21 – Touch screen connector P502

5.10. IDE/CompactFlash-Interface

The IDE interface will allow a standard connection to an external, ATAPI compliant device. That is to say, the IDE interface can be connected to off the shelf CD-ROM, DVD-ROM and hard disk drives. The IDE interface provided on the EDB9315 supports the following operating modes:

- PIO Mode 4
- Ultra DMA Mode 2

The IDE interface supports 2 external devices on a single connector, one configured as master the other as slave. Alternatively one external device may be replaced by an on board pluggable CompactFlash card. The IDE Interface supports only 16bit devices.

The IDE interface provides the following jumper configuration options:

Configuration Options

Jumper	Configuration	Remarks
J1	Pin 2-4 open = on board CompactFlash is slave Pin 2-4 closed = on board CompactFlash is master	don't care if only external devices are connected.

Table 22 – IDE Configuration Options

Device Connection

External IDE devices are connected through the standard 2x22 pin header P7.
A Compact Flash card may be directly plugged in the on-board Compact Flash connector P300.

Pin Number	Signal	Pin Number	Signal
1	RST*	2	GND
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HD0	18	HD15
19	GND	20	nc
21	nc	22	GND

23	HIOW*	24	GND
25	HIOR*	26	GND
27	IOCHRDY	28	GND
29	nc	30	GND
31	IRQ	32	IOCS16*
33	HA1	34	PDIAG*
35	HA0	36	HA2
37	HCS0*	38	HCS1*
39	DASP*	40	GND
41	+3.3V	42	+3.3V
43	GND	44	nc

Table 23 – IDE Connector P7 (2x22 pin)

Important Notes

Do not connect 2 external devices and a Compact Flash card together. This may damage the system and the IDE devices.

5.11. Serial Ports – COM1 & COM2

Two serial ports are available. Serial Port COM1 is a RS232 port with handshake signals. COM2 can be assembled as RS232 or RS485 port and does **not** support handshake signals. RS232 is the standard assembly for COM2.

The serial ports can be programmed by accessing the UART system registers in the "CPU Configuration Register" address space. See the EP9315 datasheet for details on programming the serial ports. Please note that UART2 is not functional on the IPC/NETARM boards.

Important Note

COM1 equals **UART1**, but **COM2** equals **UART3** in the EP9315 datasheet.

Device Connection

The Serial Port COM1 (UART1) is available on the internal header P5.
The Serial Port COM2 (UART3) is available on the internal header P6.

COM1 RS232

Pin Number	Signal	Pin Number	Signal
1	DCD*	2	DSR*
3	RXD	4	RTS*
5	TXD	6	CTS*
7	DTR*	8	RI*
9	GND	10	+5V (not fused)

Table 24 – RS232 Serial Port COM1 P5 (2x5 pin)

COM2 RS232 (STANDARD ASSEMBLY)

Pin Number	Signal	Pin Number	Signal
1	Nc	2	Nc
3	RXD	4	Nc
5	TXD	6	Nc
7	Nc	8	Nc
9	GND	10	+5V (not fused)

Table 25 – RS232 Serial Port P6 (2x5 pin)

COM2 Option RS485 (half duplex, no galvanic isolation)

Pin Number	Signal	Pin Number	Signal
1	Nc	2	Nc
3	RS485-	4	Nc*
5	Nc*	6	Nc*
7	Nc*	8	RS485+
9	GND	10	+5V (not fused)

Table 26 – RS485 Serial Port COM2 P6 (2x5 pin)

5.12. Keyboard PS/2 Interface

The NETARM does not provide a dedicated hardware PS/2 keyboard controller. PS/2 functionality is emulated with the SPI serial input and output of the EP9315 processor. Keyboard and Mouse functionality must be programmed in software. A keyboard driver sample code is available under Linux and Windows CE.

PS/2 signal	Processor Pin Name	Pin Number
Keyboard/ Mouse Data	SSPRX1	U14
Keyboard/ Mouse Clock	SSPTX1	V15

Table 27 – PS/2 Processor Pin Mapping

The keyboard signals are available on the MiniDIN connector P3 for direct connection of a PS/2 style keyboard or mouse. The following configuration options are provided:

Configuration Options

Jumper	Configuration	Remarks
P4	Pin 1-3, 2-4 closed = Keyboard/Mouse signals on P3	

Table 28 – PS/2 Configuration Options

Device Connection

The standard PS/2 connector P3 is used for direct connection of either a keyboard or a Mouse. The signals are directly connected to the CPU's SPI port and the PS/2 protocol (Keyboard or Mouse) must be programmed in software. The Keyboard/Mouse signals are also available on the internal 2x5 pin header P4.

Pin Number	Signal	Remarks
1	KBDATA / MDATA	
2	- (Boot Mode Pin BM1)	do not connect
3	GND	
4	+5V (not fused)	
5	KBCLK / MCLK	
6	- (Boot Mode Pin BM0)	do not connect

Table 29 – PS/2 Connector P3 (MiniDin)

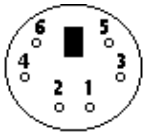

Figure 7 – MiniDin PS/2 Connector

Pin Number	Signal	Pin Number	Signal
1	KBDATA	2	KBCLK
3	P3-1	4	P3-5
5	MDATA	6	MCLK
7	BM1 / P3-2	8	BM0 / P3-6
9	GND	10	+5V (not fused)

Table 30 – PS/2 internal header P4 (2x5 pin)

Important Note

Do not connect the Boot Mode Pins on P3 or P4. These signals may only be used by the Boot Loader Key to start the Boot Loader.
The Boot Loader Key (BOOTPLUG) shortens Pin 3 and 6 of P3.

Important Note

Maximum cable length allowed for keyboard and mouse connection is 3 m.
Use shielded cables for maximum EMI protection.

5.13. 4x4 Keypad Interface

A 4x4 Keypad (or some simple switches) may be connected to the IPC/NETARM-1A Keypad Interface Port. The Keypad port of the EP9315 processor has a hardware de-bouncing capability included.

Pin Number	Signal	Remarks
1	ROW0	
2	ROW1	
3	ROW2	
4	ROW3	
5	COL0	
6	COL1	
7	COL2	
8	COL3	

Table 31 – 4x4 Keypad connector P200 (1x8 pin)

A 4x4 switch array is supported on the IPC/NETARM-1A (the EP9315 contains a 8x8 switch array capability). If the system does not use a keypad, the ROW and COL pins can be remapped to General Purpose Input/Output (GPIO) pins.

5.14. USB Interface

The NETARM-1A features an OHCI compatible USB Hostcontroller.

Device Connection

The USB interface uses two 4pin headers for the two USB channels.

P14 Pin Number	USB channel 0 Signal	P15 Pin Number	USB channel 1 Signal
1	VBUS	1	VBUS
2	D-	2	D-
3	D+	3	D+
4	GND	4	GND

Table 32 – USB Interface Connectors P14/P15 (1x4/1x4 pin)

5.15. Audio Interface

The NETARM is shipped with a standard AC-97 Audio codec.

- AC '97 2.1 Compatible
- 20-bit Stereo Digital-to-Analog Converters
- 18-bit Stereo Analog-to-Digital Converters
- Sample Rate Converter
- Extensive Power Management Support
- Headphones Stereo Output (30 Ohms minimal headphones impedance)
- Stereo Line Input
- Stereo Line Output
- Microphone Input with BIAS Voltage

Pin Number	Signal	Pin Number	Signal
1	+5V analog (250mA max. current)	2	GND
3	Mic IN	4	Mic BIAS
5	Headphones OUT R	6	Headphones OUT L
7	Line IN R	8	Line IN L
9	Line OUT R	10	Line OUT L

Table 33 – Audio Interface Connector P300 (2x5 pin 2.0mm)

5.16. Ethernet Interface

The Ethernet interface features two LED's (yellow and green) integrated into the RJ45 connector. The yellow LED on the front panel indicates Line Activity (flashing) and the green LED indicates Good Link (on).

Device Connection

The Ethernet interface uses the standard RJ45 connector P10 for 100Ω shielded or unshielded Twisted Pair cabling.

Pin Number	Signal	Remarks
1	TX+	
2	TX-	
3	RX+	
4-5	line termination	
6	RX-	
7-8	line termination	

Table 34 – Ethernet RJ45 Connector P10

5.17. Watchdog

The watchdog timer is configurable for 100 ms or 1.6 s timeout. Once timed out, it may activate the NETARM's hardware reset or the processors NMI line depending on the board system register configuration.

Configuration Options

Jumper	Configuration	Remarks
J1	Pin 4-6 open = 1.6 s Pin 4-6 closed = 100 ms	

Table 35 – Watchdog Configuration Options

The programmable logic devices on the NETARM board are factory programmed using some pins of the internal header J1. These pins **must not** be connected by the user.

Pin Number	Signal	Remarks
1	TCK	do not use
3	TDO	do not use
5	TMS	do not use
7	TDI	do not use

Table 36 – Factory Programming Header J1 (2x5 pin)

The battery backup supply for the onboard Real Time Clock and SRAM must be connected to connector P11 as follows:
(also see Table 44 – PC/104 Bus Connectors PA/PB, PC/PD

Pin Number	Signal	Remarks
1	GND	
2	no connection	
3	no connection (KEY)	
4	Vbatt	

Table 37 – External Battery Connector P11 (1x4 pin)

The user programmable output signals STOP* and TRIGGER* are available on connector P12. The signal levels are TTL compatible with maximum 4 mA sink and 2 mA source output current (also see Table 44 – PC/104 Bus Connectors PA/PB, PC/PD

Pin Number	Signal	Remarks
1	GND	
2	+5V	max. 10 mA
3	TRIGGER*	
4	STOP*	

Table 38 – User Programmable Output Connector P12 (1x4 pin)

The TRIGGER* signal may be controlled by software or by a hardware timer, i.e. Real Time Clock (32kHz) output.

6 Technical Data

6.1. Electrical Data

Important Note

Do not operate the NETARM board outside of the recommended operating conditions. Otherwise lifetime and performance will degrade. Operating the board outside of the absolute maximum ratings may damage the hardware.

Absolute Maximum Ratings (over free-air temperature range)

Parameter	Symbol	min	Nom	max	Unit
internal power supply voltage	Vcc	-0.5		5.5	Vdc
isolation logic to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation RJ45 to logic (AC, 60s, 500m a.s.l., Ta=25°C)		1500			Vrms
isolation RJ45 to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		1000			Vdc
creepage distances:					
logic to chassis and PCB border		1.0			mm
logic to PC/104 mounting holes		0.5			mm
RJ45 to logic		2.5			mm
RJ45 to chassis and PCB border		2.0			mm
storage temperature range	Tst	-40		90	°C

Table 39 – Absolute Maximum Ratings

Recommended Operating Conditions

Parameter	Symbol	min	nom	max	
logic supply voltage	Vcc	4.75	5.00	5.25	Vdc
battery backup voltage (Io=100µA)	Vbatt	2.70	3.60	3.70	Vdc
PS/2 connector (P3/P4) power load (+5V)	Ips2			200	mA
operating free-air temperature range (standard products IPC/NETARM-1A)	Ta	0		70	°C
operating free-air temperature range (extended range products IPC/NETARM–1AE)	Ta	-40		85	°C

Table 40 – Recommended Operating Conditions

Electrical Characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	typ	max	Unit
logic supply current (Vcc=5.0V, Ethernet, VGA, USB keyboard)	Icc		0.58	0.7	A
power dissipation	P		2.9	3.5	W
Vbatt loading (Vcc=0V, without SocketMemory)	Ibat(off)		2.6	3.0[1]	uA
Vbatt loading (Vcc=5V)	Ibat(on)		1.6	2.0	uA
LOWBAT* trip point		2.35	2.5	2.65	V

Table 41 – Electrical Characteristics

[1] During power cycles (Vcc transition), the Vbatt load current may shortly rise up to 13uA.

Switching Characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	nom	max	
processor clock (NETARM-1A commercial)	Fclk			200	MHz
processor clock (NETARM-1AE industrial)	Fclk			184	MHz
COM1/2 baud rate				115.2	kbaud
Watchdog timeout (short period)	Tw	70	100	140	ms
Watchdog timeout (long period)	Tw	1.0	1.6	2.25	s
Real Time Clock base clock	RTCclk		32.768		kHz
Real Time Clock accuracy (25°C)				+/-20	ppm
Real Time Clock temperature coefficient				-0.04	ppm/(°C)
Real Time Clock aging				+/-3	ppm/year

Table 42 – Switching Characteristics

6.2. Mechanical Data

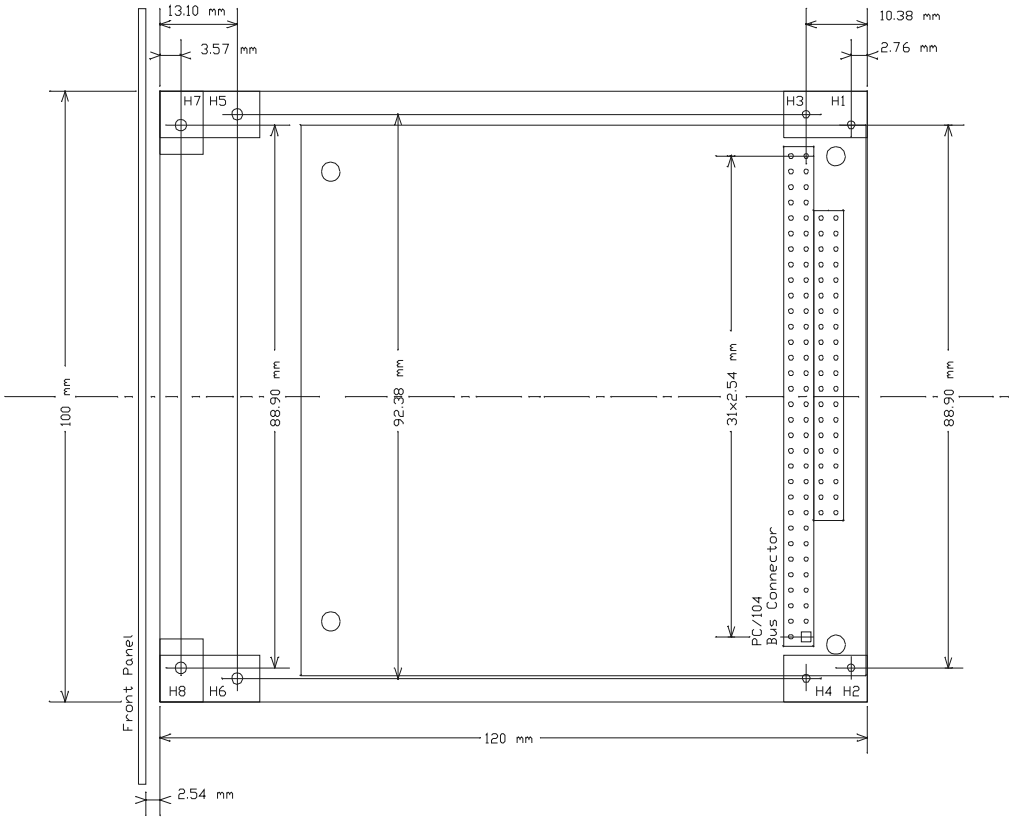

Figure 8 – Mechanical Outline

6.3. Hardware Revision State

This paragraph lists the different hardware revisions of the NETARM boards delivered beginning with the first production lot. Note that prototyping boards are not included and must be returned to factory for upgrade or replacement. All information listed in this document relies on definitive state hardware. Therefore this information may be incompatible with the prototyping board hardware.

Board Identification (see product label)	Product Revision	Remarks
IPC/NETARM-1A	#1	Original Release
IPC/NETARM-1A	#2	Layout G2639R4
IPC/NETARM-1AE	#1	Original Release

Table 43 – Hardware Revision State

Important Note

This document always covers the latest product revision listed in Table 42.
Please contact the manufacturers technical support for upgrade options.

7 Software

7.1. Operating System Support

Please contact Syslogic for the current status of operating systems support. Most common operating systems for the IPC/NETARM are the following:

	Embedded Linux (Kernel 2.6.8.1 or 2.6.20)
	Microsoft Windows CE 5.0 Real Time Operating System
	ECOS 2.0 Real Time Operating System

Syslogic does provide drivers and sample code for the IPC/NETARM.

8 References

[1] EP9315 User's Guide
(Revision 3/2004)
http://www.cirrus.com/en/pubs/manual/EP9315_Users_Guide.pdf

[2] EP9315 Datasheet
(Revision 3/2005)
http://www.cirrus.com/en/pubs/proDatasheet/EP9315_PP4.pdf

9 General Remarks

9.1. Disclaimer

The content and presentation of this document has been carefully checked. No responsibility is accepted for any errors or omissions in the documentation. Note that the documentation for the products is constantly revised and improved. The right to change this documentation at any time without notice is therefore reserved. Syslogic is grateful for any help referring to errors or for suggestions for improvements.

The following registered trademarks are used:

PS/2	trademarks of IBM Corporation
I^2C	trademark of Philips Corporation
CompactFlash	trademark of SanDisk Corporation
DiskOnChip	registered trademark of M-Systems LTD
PC/104	trademark of PC/104 Consortium
NETARM	trademarks of Syslogic Datentechnik AG
ARM	trademark of Advanced RISC Machines Corp.

9.2. Contents of this Documentation

This document addresses to system integrators, programmers and instructed installation and maintenance personal working with the PC/104 system. It provides information needed to setup and program the IPC/NETARM-1A processor boards. For complete information also the documentation of the mounted communications and I/O boards must be consulted.

9.3. Additional Products and Documents

9.3.1. Hardware Products

The following hardware products are useful together with the NETARM processor board:

- NETARM boot loader key (CUB/BOOTPLUG-1A, part of CUB/DOWNKIT-1A)
- NETARM serial port cable (AT-Link cable, part of CUB/DOWNKIT-1A)
- PC/104 communication boards (see product catalog)
- PC/104 I/O boards (see product catalog)

9.3.2. Software Products

The following software products are useful together with the NETARM processor board:

- IPC/CRATER-10A: Embedded Linux Distribution for NETARM boards
- IPC/WINCE-50A: Windows CE 5.0 for NETARM boards

9.3.3. Documents

The following documents are *required* for correct installation and operation of the NETARM processor board:

- DOC/CUBINST: User Documentation for FBCube Installation
  Note : also contains the necessary information related to the “ce”-certification of the products
- DOC/NETARMFW: User Documentation for NETARM Firmware

The following documents are *useful* for additional information about PC/104 and IEEE 996.1:

- PC/104 Specification Version 2.3
- IEEE 996: IEEE standard document ‘Personal Computer Bus Standard’
- IEEE 996.1: IEEE standard document ‘Compact Embedded-PC Modules’
- ISBN 0-929392-15-9: ‘ISA & EISA, Theory and Operation’ by Edward Solari (Annabooks, San Diego)

The PC/104 Specification may be downloaded from the Internet (see address below).

- PC/104 Consortium
  www.pc104.org

The IEEE standard documents may be ordered directly from the IEEE or any standards document distributor (see addresses below).

- IEEE Standards Department
  www.ieee.org
- Global Engineering Documents
  www.global.ihs.com

9.4. Items delivered

The NETARM comes without cabling and enclosure. These additional items must be ordered separately and installed according to the respective user documentations. A standard configuration based on the NETARM processor board could be as follows:

- PC/104 power supply board
- PC/104 processor board IPC/NETARM-1A
- enclosure
- Cabling for two serial ports and mouse port
  Note : Mounting procedure is described in DOC/CUBINST

9.5. CE certification of the board

The IPC/NETARM conforms to the following standards in accordance with the *industrial environment* class specification of the device.

EN 55022:2006:
Information technology equipment – Radio disturbance characteristics – Limits and methods of measurement

EN 55024:1998 + A1:2001 + A2:2003:
Information technology equipment – Immunity characteristics – Limits and methods of measurements

EN 61000-6-2:2005:
Electromagnetic compatibility (EMC) Part 6-2: Generic standards – Immunity for industrial environments

Note: The immunity requirements in EN 61000-6-2 are higher than those in EN 55024; by accomplishing the generic standard EN 61000-6-2 the product standard EN 55024 is also accomplished.

EN 50121-3-2:2006:
Railway applications – Electromagnetic compatibility – Part 3-2: Rolling stock – apparatus

EN 55011:2007 + A2:2007:
Industrial scientific and medical (ISM) radio-frequency equipment – Electromagnetic disturbance characteristics – Limits and methods of measurement

9.6. Installation

The installation of the NETARM board is described in the documentation DOC/CUBINST. The firmware configuration and download is described in the appropriate firmware documentation.

Important Note

Before applying power to the NETARM system, all installed boards must be correctly configured and mounted (please consult the corresponding User Documentations).

9.7. Safety Recommendations and Warnings

The product is intended for measurement, control and communications applications in industrial environments. The product must be assembled and installed by specially trained people. The strict observation of the assembly and installation guidelines is mandatory. The use of the product in systems in which life or health of persons is directly dependent (e.g. life support systems, patient monitoring systems, etc.) is not allowed. The use of the product in potentially explosive atmospheres requires additional external protection circuitry which is not provided with the product. In case of uncertainty or of believed errors in the documentation please immediately contact the manufacturer. Do not use or install the product if you are in doubt. In any case of misuse of the product, the user is solely liable for the consequences.

9.8. Life Cycle Information

9.8.1. Transportation and Storage

During transportation and storage the product must be in its original packing. The original packing contains an antistatic bag and shock-absorbing material. It is recommended, to keep the original packing in case of return of the product to the factory for repair. Note that the packing is recyclable.

9.8.2. Assembly and Installation

Observe the EMI-precautions against static discharge. Carefully read the assembly and installation documentation (Document DOC/CUBINST) before unpacking the product. Make sure that you have all the necessary items ready (including all the small parts). Follow the assembly guidelines in DOC/CUBINST strictly. Note that deviations from the installation guidelines may result in degraded operational reliability or in unfavourable EM-radiation or EM-susceptibility.

9.8.3. Operation

The operating environment must guarantee the environmental parameters (temperature, power supply, etc.) specified in the technical specification section of the product manual. The main functionality of the IPC system is defined by the application programs running on the processor board. The application programs are not part of the delivery by Syslogic but are defined, developped and tested by the customer or a system-integrator for each specific application. Refer to the respective documentation for more information.

9.8.4. Maintenance and Repair

The IPC system features error- and malfunction-detection circuitry. Diagnostic information gathered is transferred to the applications software where it can be used. In the rare case of a module hardware-failure or malfunction, the complete board should be exchanged. The faulty board must be returned to the factory for repair. Please use whenever possible the original packing for return of the product (EMI and mechanical protection).

9.8.5. Disposal

At the end of the lifespan the IPC products must be properly disposed. IPC products contain a multitude of elements and must be disposed like computer parts. Some of the IPC products contain batteries which should be properly disposed.

10 Manufacturer Information

10.1. Contact

Our distributors and system integrators will gladly give you any information about our products and their use. If you want to contact the manufacturer directly, please send a fax or email message containing a short description of your application and your request to the following address or use one of the information or technical support request forms on our internet homepage:

Syslogic Datentechnik AG
Täfernstrasse 28
CH-5405 Baden-Dättwil / Switzerland

Email: info@syslogic.ch
www: http://www.syslogic.ch
Fax: +41 (0)56 200 90 50

Technical support:
support@syslogic.ch

10.2. Warranty

Our products are covered by a world-wide manufacturers warranty. The warranty period starts at the delivery time from our official distributor to the customer. The duration of the warranty period is specified in the respective product catalogs and the offers. All products carry a job number for identification. The manufacturing data and deliveries are registered in a high level Quality Management System.
The warranty covers material and manufacturing defects. All products must be returned via the official distributor to the factory for repair or replacement. The warranty expires immediately if the products are damaged of operation outside of the specified recommended operating conditions. The warranty also expires if the date code or job number listed on the product is altered or rendered unintelligible. The warranty does not include damage due to errors in firmware or software delivered with the products.

APPENDIX A – PC104 Bus Connector

Pin		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*
						A1	⊗	IOCHCK#	B1	⊗	GND
P11			P12			A2	⊗	SD7	B2	⊗	RESETDRV
1	⊗	GND	1	⊗	GND	A3	⊗	SD6	B3	⊗	+5V
2	⊗	no connection	2	⊗	+5V	A4	⊗	SD5	B4	⊗	IRQ9
3	⊗	no connection	3	⊗	TRIGGER*	A5	⊗	SD4	B5	⊗	-5V (not used)
4	⊗	Vbatt	4	⊗	STOP*	A6	⊗	SD3	B6	⊗	DRQ2
						A7	⊗	SD2	B7	⊗	-12V (not used)
						A8	⊗	SD1	B8	⊗	0WS#
D0	⊗	GND	C0	⊗	GND	A9	⊗	SD0	B9	⊗	+12V (not used)
D1	⊗	MEMCS16#	C1	⊗	SBHE#	A10	⊗	IOCHRDY	B10	⊗	(KEY)
D2	⊗	IOCS16#	C2	⊗	LA23	A11	⊗	AEN	B11	⊗	SMEMW#
D3	⊗	IRQ10	C3	⊗	LA22	A12	⊗	SA19	B12	⊗	SMEMR#
D4	⊗	IRQ11	C4	⊗	LA21	A13	⊗	SA18	B13	⊗	IOW#
D5	⊗	IRQ12	C5	⊗	LA20	A14	⊗	SA17	B14	⊗	IOR#
D6	⊗	IRQ15	C6	⊗	LA19	A15	⊗	SA16	B15	⊗	*DACK3#* [2]
D7	⊗	*IRQ14* [2]	C7	⊗	LA18	A16	⊗	SA15	B16	⊗	*DRQ3* [2]
D8	⊗	*DACK0#* [2]	C8	⊗	LA17	A17	⊗	SA14	B17	⊗	*DACK1#* [2]
D9	⊗	*DRQ0* [2]	C9	⊗	MEMR#	A18	⊗	SA13	B18	⊗	*DRQ1* [2]
D10	⊗	*DACK5#* [2]	C10	⊗	MEMW#	A19	⊗	SA12	B19	⊗	REFRESH#
D11	⊗	*DRQ5* [2]	C11	⊗	SD8	A20	⊗	SA11	B20	⊗	SYSCLK
D12	⊗	*DACK6#* [2]	C12	⊗	SD9	A21	⊗	SA10	B21	⊗	IRQ7
D13	⊗	*DRQ6* [2]	C13	⊗	SD10	A22	⊗	SA9	B22	⊗	IRQ6
D14	⊗	*DACK7#* [2]	C14	⊗	SD11	A23	⊗	SA8	B23	⊗	IRQ5
D15	⊗	*DRQ7* [2]	C15	⊗	SD12	A24	⊗	SA7	B24	⊗	*IRQ4* [2]
D16	⊗	+5V	C16	⊗	SD13	A25	⊗	SA6	B25	⊗	*IRQ3* [2]
D17	⊗	MASTER#	C17	⊗	SD14	A26	⊗	SA5	B26	⊗	DACK2#
D18	⊗	GND	C18	⊗	SD15	A27	⊗	SA4	B27	⊗	TC
D19	⊗	GND	C19	⊗	(KEY)	A28	⊗	SA3	B28	⊗	BALE
						A29	⊗	SA2	B29	⊗	+5V
						A30	⊗	SA1	B30	⊗	OSC
						A31	⊗	SA0	B31	⊗	GND
						A32	⊗	GND	B32	⊗	GND

Table 44 – PC/104 Bus Connectors PA/PB, PC/PD

[2] These pins/signals are not implemented on the IPC/NETARM PC/104 bus.
(IRQ channels 3,4,14 and DMA channels 0,1,3,5,6,7)

Important Note

For proper operation ***all*** +5V and GND pins must be connected with short, low impedance lines to the main power supply.

Important Note

Do not connect bus drivers/receivers with integrated bushold circuit to the PC/104 signals. This may disturb proper operation of the NETARM board or add-on boards.

APPENDIX B – MISC.

10.3. Pulse Width Modulator

Brightness control for the TFT panel can be programmed by setting up the BRIGHT register (see chapter 7 of EP9315 User's Guide).

Brightness control for the Character LCD can be programmed by setting up the PWM registers of the EP9315 chip (see chapter 24 of EP9315 User's Guide).