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IPC/SL8xxx-AxxxE, IPC/ML8xxx-AxxxE

Document Ordercode: DOC/IPC_SL8-E

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1.0	05.06.2015	U. Müller	Release
1.1	02.05.2016	U. Müller	added product types with CAN and RS485
1.2	17.10.2016	U. Müller	added USB current limit values
1.3	13.06.2017	U. Müller	added BIOS CMOS setting for RS485/RS422
1.4	04.08.2017	U. Müller	updated errata list
1.5	15.12.2017	U. Müller	added backup time, corrected LVDS signals
1.6	05.06.2018	U. Müller	added CAN isolation data
1.7	20.06.2018	J. Berner	Adapted PCU timing configuration table (S14)
1.8	26.04.2019	D. Lagler	Added variant with LTE/GPS
1.9	01.07.2019	J. Berner	Added workaround for SDCard Interface bug.

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1 Introduction

1.1. General Remarks

The content and presentation of this document has been carefully checked. No responsibility is accepted for any errors or omissions in the documentation.

Note that the documentation for the products is constantly revised and improved. The right to change this documentation at any time without notice is therefore reserved.

Syslogic is grateful for any help referring to errors or for suggestions for improvements.

The following registered trademarks are used:

IBM-PC, PC/AT, PS/2	trademarks of IBM Corporation
I²C	trademark of Philips Corporation
CFast	trademark of CompactFlash Association
PC/104	trademark of PC/104 Consortium
PCIe	trademark of PCI-SIG

1.2. Contents of this Documentation

This document addresses to system integrators, programmers and instructed installation and maintenance personal working with the industrial PC system. It provides all information needed to configure, setup and program the IPC/SL8xxx-AxxxE systems. For complete information also the documentation of the mounted communications and I/O boards must be consulted. In the following paragraphs all descriptions referenced to SL8 apply to all, the IPC/SL8-AxxxE and products, if not declared otherwise.

1.3. Additional Products and Documents

1.3.1. Hardware Products

The following hardware products are useful together with the SL8 system:
- Syslogic PC/104 communication boards (see product catalog)
- Syslogic PC/104 I/O boards (see product catalog)

1.3.2. Software Products

The following software products are useful together with the SL8 system:
- IPC/IOCOMSW-1A: Sample program code and utilities for x86 based PC/104 systems

1.3.3. Documents

The following additional documents are *useful* for correct installation and operation of the SL8 system:

 − DOC/IPC_IOCOMSW: User Documentation for programming examples and utilities

The following documents are *useful* for additional information about MiniPCIe:

 − PCIe Base Specification Version 1.1
 − PCIe Mini Card Electromechanical Specification Version 1.2

The MiniPCIe Specification may be downloaded from the Internet (see address below).

 − PCI-SIG Consortium
    www.pcisig.com/specifications/pciexpress/base

The following documents are *useful* for additional information about PC/104 and IEEE 996.1:

 − PC/104 Specification Version 2.3
 − IEEE 996: IEEE standard document 'Personal Computer Bus Standard'
 − IEEE 996.1: IEEE standard document 'Compact Embedded-PC Modules'
 − ISBN 0-929392-15-9: 'ISA & EISA, Theory and Operation' by Edward Solari (Annabooks, San Diego)

The PC/104 Specification may be downloaded from the Internet (see address below).

 − PC/104 Consortium
    www.pc104.org

The IEEE standard documents may be ordered directly from the IEEE or any standards document distributor (see addresses below).

 − IEEE Standards Department
    www.ieee.org
 − Global Engineering Documents
    www.global.ihs.com

1.4. Items delivered

The SL8 comes without external cabling and power supply. These additional items must be ordered separately and installed according to the respective user documentations.

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1.5.   Installation

The installation of the SL8 system is described in chapter 5 of this documentation.

Important Note

Before applying power to the SL8 system, all installed boards must be correctly configured and mounted.

1.6.   Safety Recommendations and Warnings

1.6.1.   General safety recommendations

The products are intended for measurement, control and communications applications in industrial environments. The products must be assembled and installed by specially trained people. The strict observation of the assembly and installation guidelines is mandatory.

The use of the products in systems in which life or health of persons is directly dependent (e.g. life support systems, patient monitoring systems, etc.) is not allowed.

The use of the products in potentially explosive atmospheres requires additional external protection circuitry which is not provided with the products.

In case of uncertainty or of believed errors in the documentation please immediately contact the manufacturer (address see chapter 10). Do not use or install the products if you are in doubt. In any case of misuse of the products, the user is solely liable for the consequences.

1.6.2.   Safety warnings

Check chapter 5 for detailed installation and cabling requirements.

Do not operate this product outside of the recommended operating conditions according to the technical data specified in paragraph 6.

Do not touch the surface of this product without precaution, it may be hot and burn your skin. Cool it down before touching.

Do not touch any connector unless you have verified that no dangerous voltage is around. Disconnect cabling first.

Do not open any part of the enclosure while power is applied.

Do not try to repair any defective product by yourself. There is no replaceable service part inside.

Do not open the service cover unless you are instructed and entitled to do this. The service cover is intended for inserting the CFast software storage card on initial operation of the product by an instructed person only.

Use an overload protected power supply to prevent damage in case of a short inside the system.

1.7. Electro-static discharge

Electronic boards are sensitive to Electro-Static Discharge (ESD). Please ensure that the product is handled with care and only in a ESD protected environment. Otherwise a proper operation is not guaranteed and the warranty is not applicable.

1.8. Life Cycle Information

1.8.1. Transportation and Storage

During transportation and storage the products must be in their original packing. The original packing contains antistatic and shock-absorbing material. It is recommended, to keep the original packing in case of return of the product to the factory for repair. Note that the packing is recyclable.

1.8.2. Assembly and Installation

Observe the EMI-precautions against static discharge. Carefully read the assembly and installation documentation (see chapter 5) before unpacking the products. Make sure that you have all the necessary items ready (including all the small parts). Follow the assembly guidelines in chapter 5 strictly.

The installation procedures must be strictly observed. Note that deviations from the installation guidelines may result in degraded operational reliability or in unfavourable EM-radiation or EM-susceptibility.

1.8.3. Operation

The operating environment must guarantee the environmental parameters (temperature, power supply, etc.) specified in the technical specification section of the product manuals.

The main functionality of the SL8 system is defined by the application programs running on the processor board. The application programs are not part of the delivery by Syslogic but are defined, developed and tested by the customer or a system-integrator for each specific application. Refer to the respective documentation for more information.

1.8.4. Maintenance and Repair

The IPC system features error- and malfunction-detection circuitry. Diagnostic information gathered is transferred to the applications software where it can be used. In the rare case of a module hardware-failure or malfunction, the complete system should be exchanged. The faulty system must be returned to the factory for repair. Please use whenever possible the original packing for return of the product (EMI and mechanical protection).

1.8.5. Disposal

At the end of the lifespan the SL8 products must be properly disposed. SL8 products contain a multitude of elements and must be disposed like computer parts. Some of the SL8 products contain batteries which should be properly disposed.

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2 Product Description

2.1. Features

The SL8 system is a x86 based industrial PC designed for use with the IPC line of communications and I/O boards. Its many different variants allow to build up various industrial controls based on the standard PC/AT architecture.

The SL8 offers the following main features:

- low power industrial processor board eliminating the need for enforced cooling
- high performance 64-bit Intel Atom based processor core with integrated floating point unit
- up to 1.9 GHz processor clock
- DDR3 DRAM memory
- up to 4 Gbyte DRAM on board
- 64-bit graphics controller with backwards compatibility to VGA and SVGA standards
- graphics controller supporting up to 1900 x 1200 dots resolution on DVI-D port
- optional LCD interface (3x8 bit LVDS)
- SATA interface supporting one CFast card socket and one standard SATA port.
- integrated peripheral controller (IPC) with PC/AT compatible DMA controllers (2 x 8237), interrupt controllers (2 x 8259) and timer/counter channels (8254)
- PC/AT compatible keyboard controller (8042)
- up to four serial RS232 ports (COM1-4) with 16 byte receive and transmit fifo (16550A)
- option of one serial ports (COM2) as galvanic isolated RS422/485 interface (half/fullduplex)
- one USB V3.0/ V2.0 port (XHCI-Hostcontroller) with Super-, High-, Full- and Low-Speed support
- three USB V2.0 ports (OHCI/EHCI-Hostcontroller) with High-, Full- and Low-Speed support
- up to two CAN 2.0b compatible standalone PCIe CAN controllers
- two 10/100/1000Mbit Ethernet LAN interfaces
- Year 2000 compliant Real Time Clock (PC/AT compatible)
- hardware watchdog configurable for 100 ms to 256 s timeout and Non-maskable Interrupt (NMI) or hardware reset activation
- temperature supervisor for software controlled power management
- Flash for BIOS and BIOS extensions
- supervised battery backup for Real Time Clock
- PC/104 bus interface for expansion with standard 8 bit I/O PC/104 communications and I/O boards
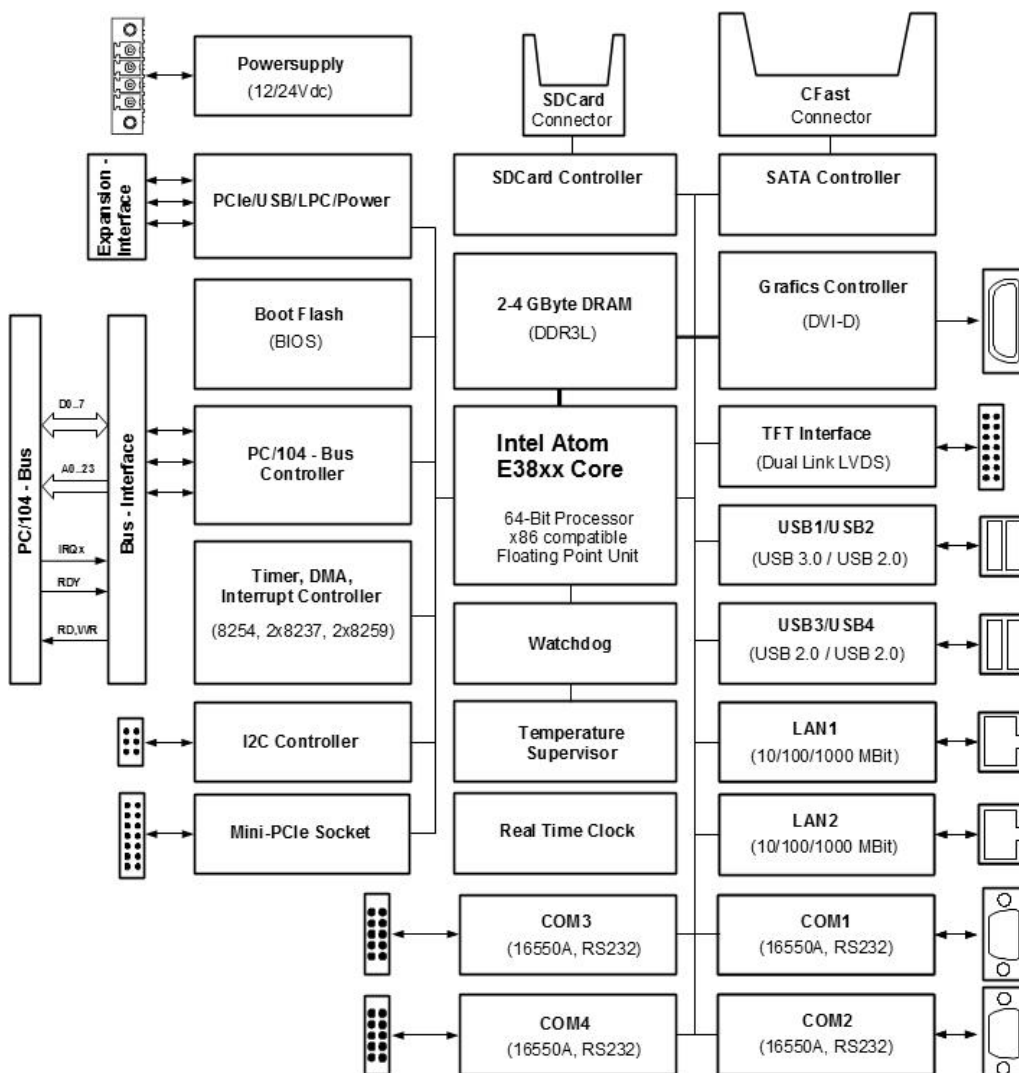
Fig. 1   Block Diagram SL8-10xE (all functions)

Important Note

Check the product variant carefully for the supported functions.
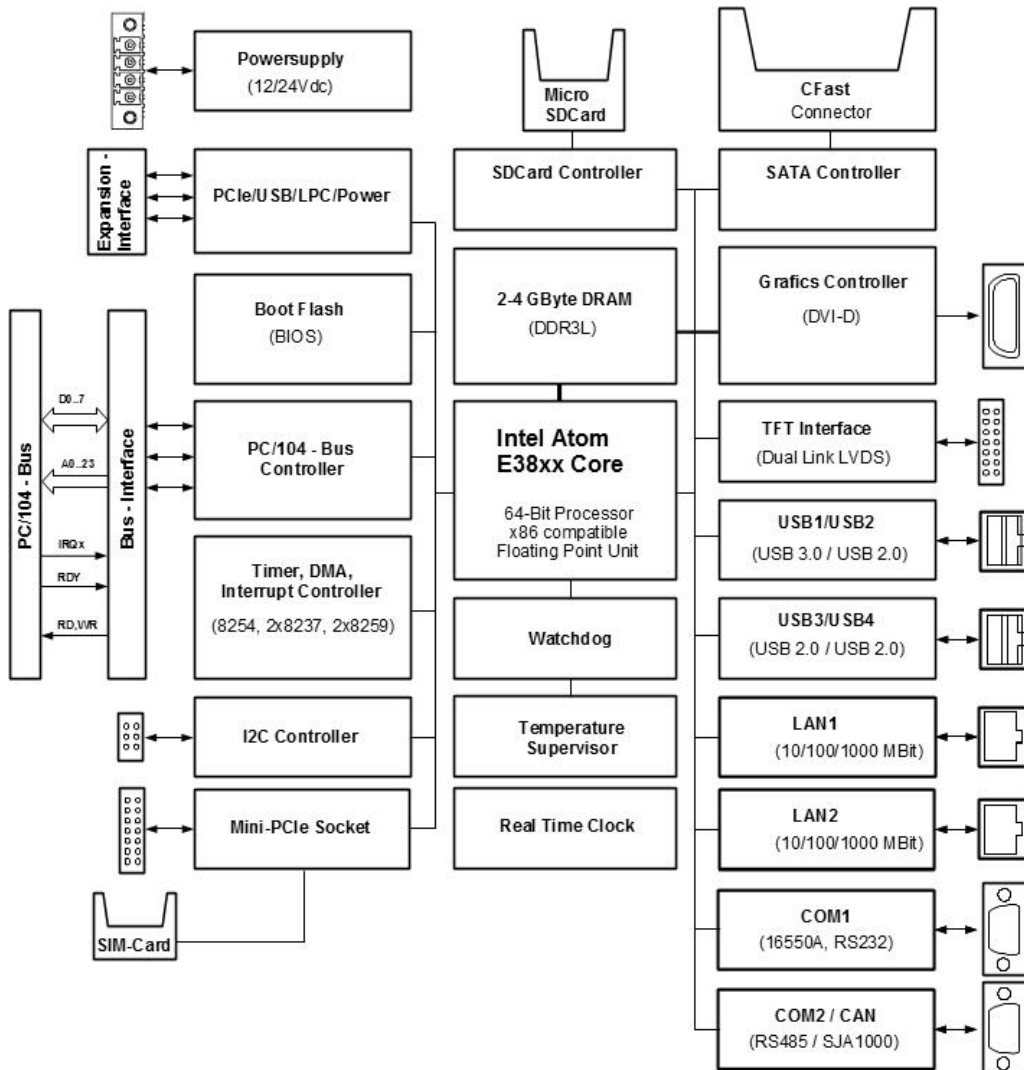
Fig. 2   Block Diagram SL8-12xE (all functions)

Important Note
Check the product variant carefully for the supported functions.

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2.2.   Product Variants

The SL8 is available in different functional variants and enclosures.

The following tables show the functional differences for the SL size enclosure and the ML size enclosure variants. Bold printed functions are available on a front or rear connector, italic printed functions are available as internal interfaces only. See figure Fig. 3 for location of the internal interfaces.

Function	IPC/SL8G13-A101E	IPC/SL8H19-A101E	IPC/SL8H19-A103E	IPC/SL8H19-A121E	IPC/SL8H19-A123E
CPU	*Atom E3825 1.3GHz*	*Atom E3845 1.9GHz*	*Atom E3845 1.9GHz*	*Atom E3845 1.9GHz*	*Atom E3845 1.9GHz*
Memory	*2 GByte*	*4 GByte*	*4 GByte*	*4 GByte*	*4 GByte*
LAN1	**LAN1**	**LAN1**	**LAN1**	**LAN1**	**LAN1**
LAN2	**LAN2**	**LAN2**	**LAN2**	**LAN2**	**LAN2**
COM1	**COM1**	**COM1**	**COM1**	**COM1**	**COM1**
COM2	**COM2 (RS232)**	**COM2 (RS232)**	**COM2 (RS232)**	*P42/RS232*	**COM2 (RS485)**
COM3	*P43/RS232*	*P43/RS232*	-	-	-
COM4	*P44/RS232*	*P44/RS232*	-	-	-
CAN1	-	-	-	**CAN**	-
USB1/2	**USB1/2**	**USB1/2**	**USB1/2**	**USB1/2**	**USB1/2**
USB3/4	**USB3/4**	**USB3/4**	**USB3/4**	**USB3/4**	**USB3/4**
USB5	*P22*	*P22*	-	*P22*	*P22*
USB6	*P23*	*P23*	-	*P23*	*P23*
LPT	-	-	-	-	-
PS/2 Keyb	-	-	-	-	-
DVI-D	**DISPLAY**	**DISPLAY**	**DISPLAY**	**DISPLAY**	**DISPLAY**
LCD LVDS	-	-	-	-	-
LCD Backlight	-	-	-	-	-
I2C	*P46*	*P46*	-	*P46*	*P46*
Audio	-	-	Buzzer	-	-
CFast	*P8*	*P8*	*P8*	*P8*	*P8*
SDCard	*P7*	*P7*	*P7*	*P7*	*P7*
Expansion Bus	-	-	-	-	-
PC/104 Slot	-	-	-	-	-
RTC Backup	Li battery	Li battery	Li battery	Li battery	Li battery

Tab. 1   Product Variants SL

Function	IPC/ML8G13-A101E	IPC/ML8H19-A101E	IPC/ML8H19-B201E	
CPU	*Atom E3825 1.3GHz*	*Atom E3845 1.9GHz*	*Atom E3845 1.9GHz*	
Memory	*2 GByte*	*4 GByte*	*4 GByte*	
LAN1	**LAN1**	**LAN1**	**LAN1**	
LAN2	**LAN2**	**LAN2**	**LAN2**	
COM1	**COM1**	**COM1**	**COM1**	
COM2	**COM2**	**COM2**	**COM2**	
COM3	**COM3**	**COM3**	**COM3**	
COM4	**COM4**	**COM4**	**COM4**	
USB1/2	**USB1/2**	**USB1/2**	**USB1/2**	
USB3/4	**USB3/4**	**USB3/4**	**USB3/4**	
USB5	*P22*	*P22*	*P22*	
USB6	*P23*	*P23*	*P23*	
LPT	-	-	-	
PS/2 Keyb	-	-	-	
DVI-D	**DISPLAY**	**DISPLAY**	**DISPLAY**	
LCD LVDS	-	-	-	
LCD Backlight	-	-	-	
I2C	*P46*	*P46*	*P46*	
Audio	*P47/P3*	*P47/P3*	*P47/P3*	
CFast	*P8*	*P8*	*P8*	
SDCard	*P7*	*P7*	*P7*	
Expansion Bus	*P51*	*P51*	*P51*	
PC/104 Slot	yes	yes	yes	
RTC Backup	Li battery	Li battery	Li battery	
ANT1	-	-	GPS	
ANT2	-	-	Cellular	
ANT3	-	-	Diversity	

Tab. 2   Product Variants ML

2.3. Operating Modes

The SL8 is based on the standard PC/AT architecture and therefore operates in DOS-compatible mode (real mode) on start up. The configurable BIOS initializes all onboard peripherals to their default values, executes the BIOS extensions programmed into the onboard BIOS-Flash and BIOS extensions found on installed expansion boards prior to booting the operating system from a user-selectable drive (boot sector). The operating system (or eventually a BIOS extension) may switch to protected mode to execute high performance 32-bit or 64-bit program code.

2.4. Startup Modes

The SL8 may startup either in normal operating mode or in BIOS recovery mode:

- BIOS recovery mode is invoked when rotary switch S1 is set to position '8'.
  In BIOS recovery mode is intended to reprogram a corrupt main BIOS. Before starting the reprogram process, switch S1 must be reset to position '0', otherwise the recovery BIOS will be overwritten.
- Normal operating mode is invoked when rotary switch S1 is set to position '0'.

Other parameters like backlight control and watchdog base timeout are also dependent on S1 setting:

Switch S1	Startup Mode	Backlight Polarity	Backlight Control	Watchdog Base Timeout
0	normal operating modes	normal	by BIOS setting	1 s
1		normal	by BIOS setting	100ms
2		normal	by PWM Register 820Dh	1 s
3		normal	by PWM Register 820Dh	100ms
4		inverted	by BIOS setting	1 s
5		inverted	by BIOS setting	100ms
6		inverted	by PWM Register 820Dh	1 s
7		inverted	by PWM Register 820Dh	100ms
8	BIOS recovery mode	normal	by BIOS setting	1 s
9	factory modes	normal	by BIOS setting	1 s
A	(do not use)	normal	by PWM Register 820Dh	1 s
B		normal	by PWM Register 820Dh	1 s
C	factory modes	inverted	by BIOS setting	1 s
D	(do not use)	inverted	by BIOS setting	1 s
E		inverted	by PWM Register 820Dh	1 s
F		inverted	by PWM Register 820Dh	1 s

Tab. 3   Startup Modes

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3 Hardware Description

3.1. Overview

The SL8 hardware may be configured by software (CMOS setup) and by switch settings. Custom BIOS configuration can be programmed into the BIOS flash on request (ask Syslogic technical support for custom BIOS configuration).

The switch and connector locations are shown in the board layout drawing (Fig. 3).

Important Note

Always check the jumper configuration of a freshly received board to comply with your system requirements before applying power, otherwise the system may get damaged or may fail to operate.

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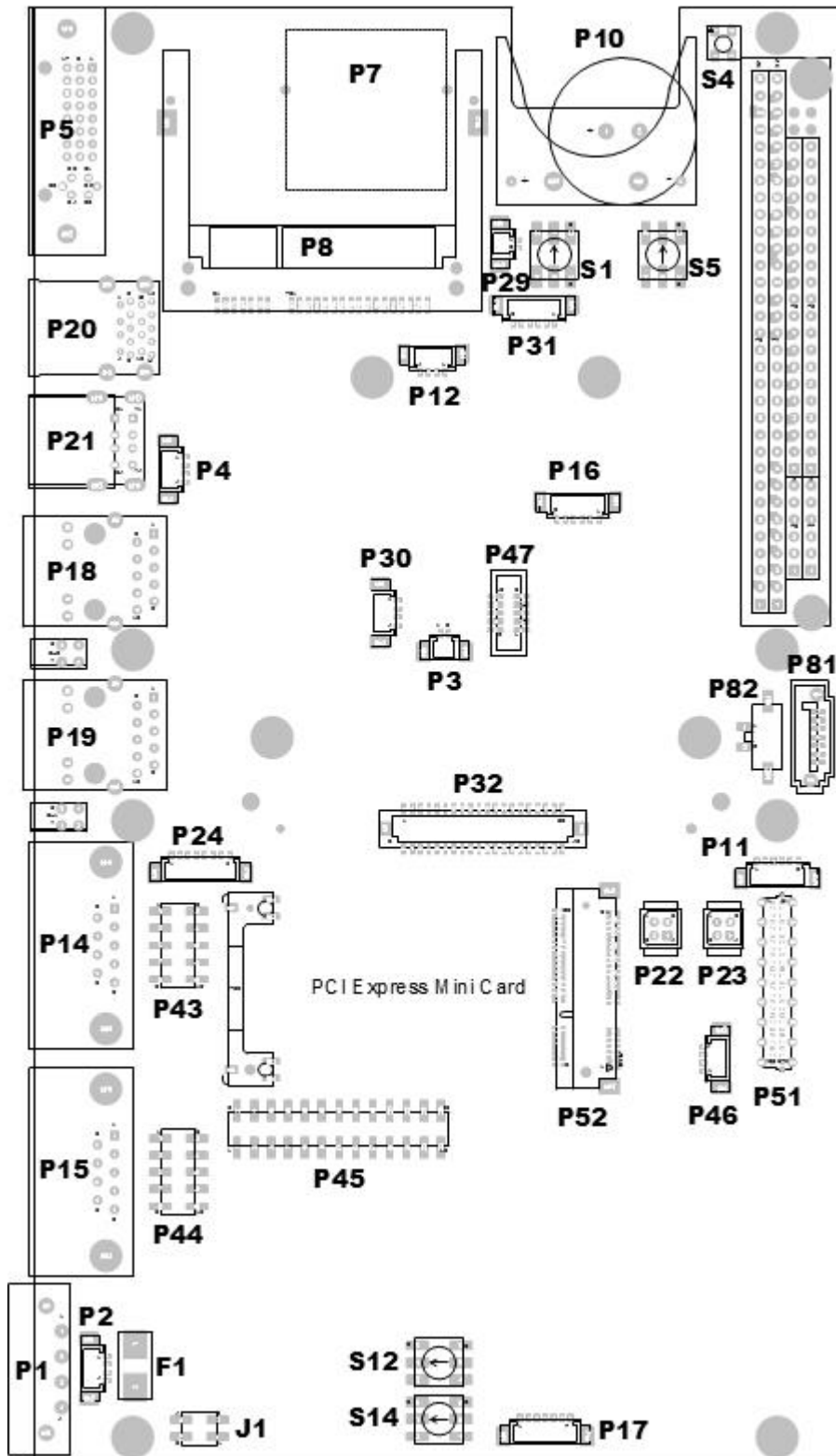
Fig. 3   Board Layout SL8-10xE (all functions)

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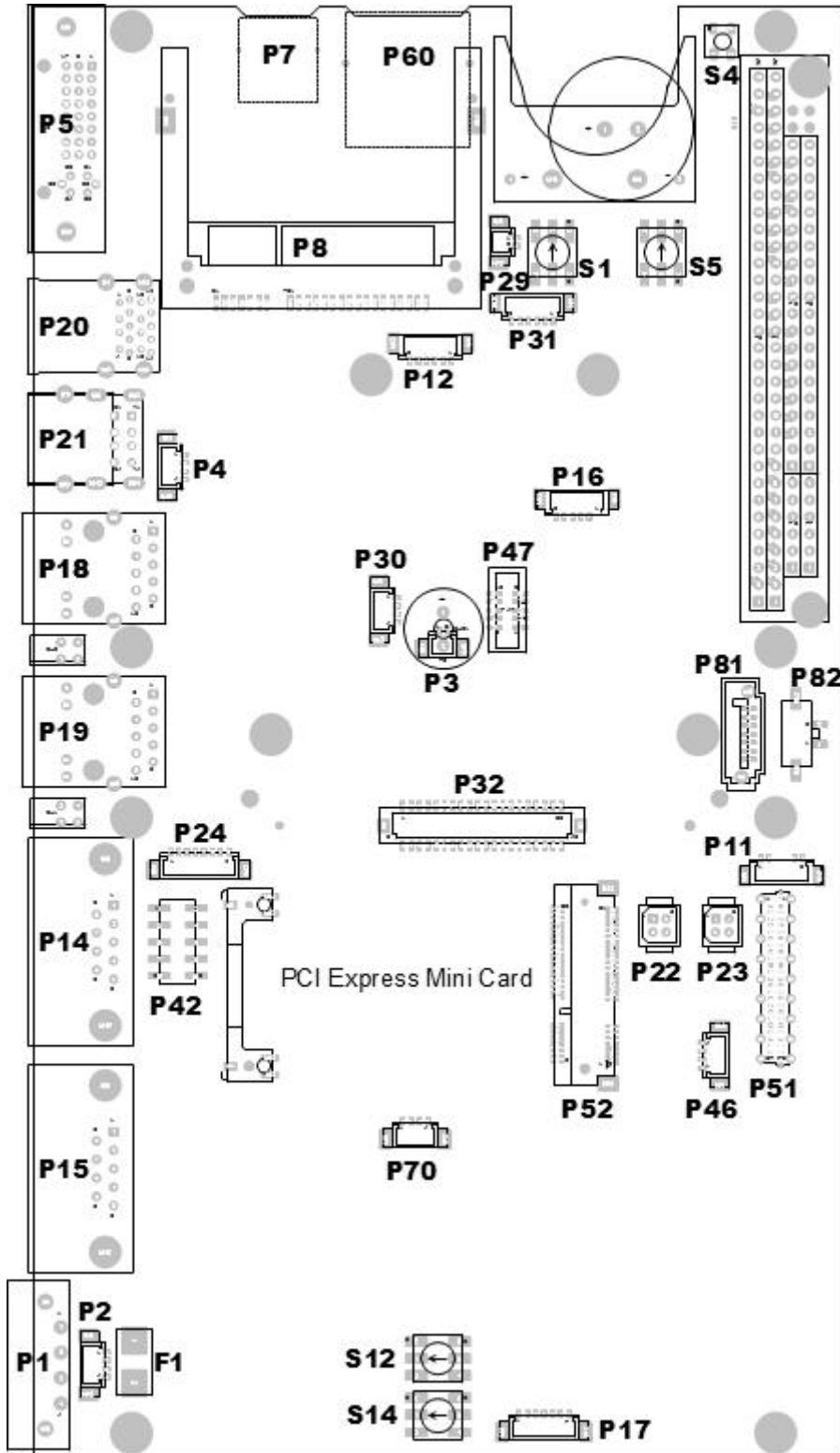
Fig. 4   Board Layout SL8-12xE (all functions)

3.2. Memory and I/O Resources

3.2.1. General Memory Layout and Configuration

The SL8 uses the same memory layout as a standard desktop PC. Three onboard devices , DRAM, graphics controller, and BIOS, make use of the 4 Gbyte (32-bit mode) / 64Gbyte (64-bit mode) adressable memory space.

Address	Device / Register	Remarks
0000'0000..0009'FFFFH	640 kbyte Main Memory (DRAM)	
000A'0000..000B'FFFFH	VGA Video Memory	
000C'0000..000F'FFFFH	Configurable memory range (BIOS, BIOS Extensions, DRAM or redirected to PC/104 bus)	
0010'0000.. FFFF'FFFFH	2-4 Gbyte Main Memory (DRAM)	including graphics memory (UMA)
0000'0001'0000'0000.. 0000'0001'FFFF'FFFFH	optional 4 Gbyte Main Memory (DRAM)	64-bit mode only
0000'0002'0000'0000.. 0000'000F'FFFF'FFFFH	up to top	64-bit mode only

Tab. 4   Physical Memory Address Space Layout

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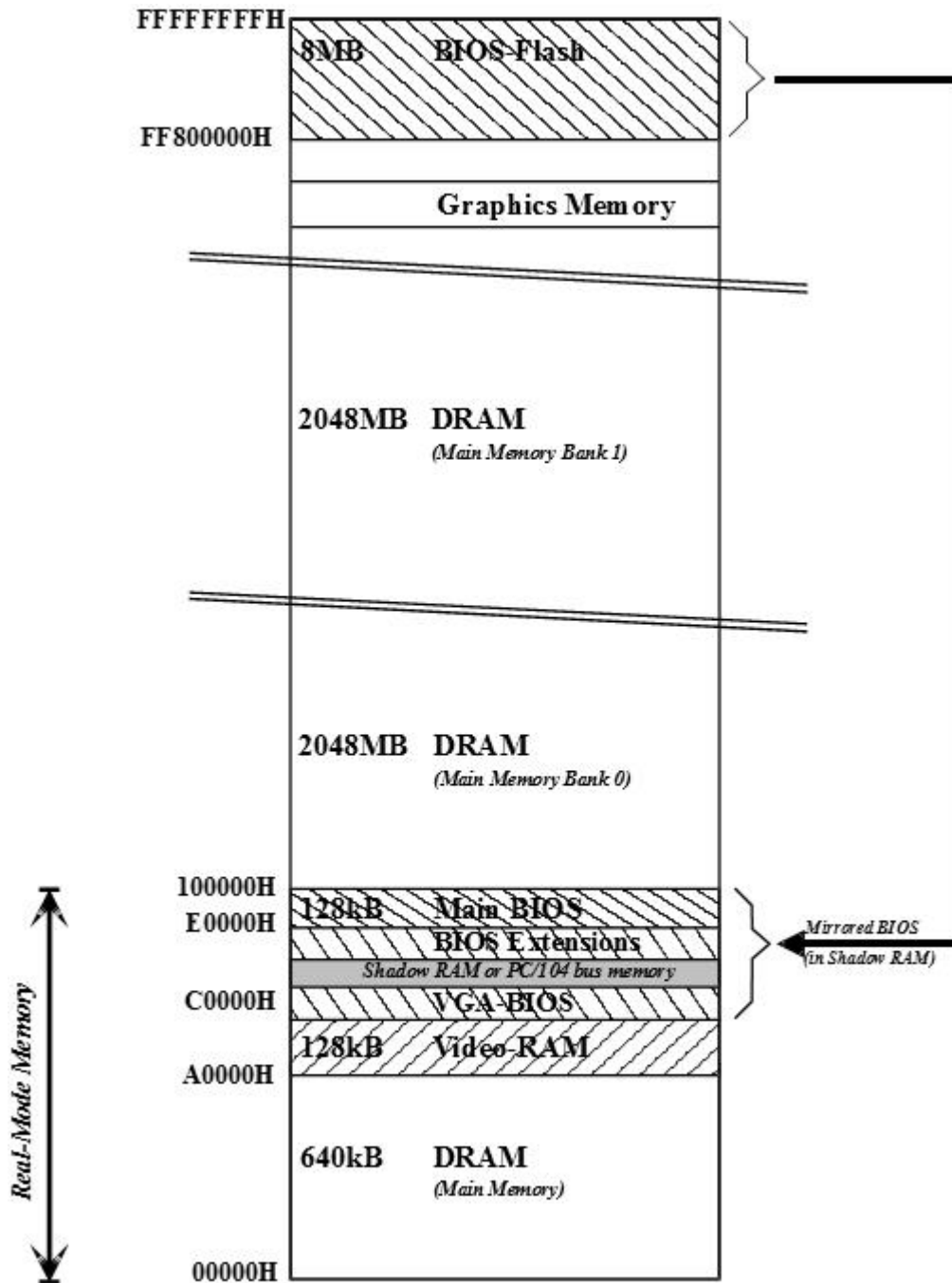
Fig. 5   Memory Map

3.2.2. General I/O Layout and Configuration

The SL8's 64 kbyte I/O address space is mapped to the PC/104 bus address space as indicated in the table below. Note that 16 bit address decoding should be used on all PC/104 expansion boards to make efficient use of the I/O address space.

Address	Device / Register	Remarks
0000..001FH	DMA Controller 1	
0020..0021H	Master Interrupt Controller	
0022H	Configuration Address Register	
0023H	Configuration Data Register	
0024..003FH	reserved	
0040..0043H	Timer/Counter	
0044..005FH	reserved	
0060H	Keyboard/Mouse Controller	
0061H	Port B Register	
0062..0063H	reserved	
0064H	Keyboard/Mouse Controller	
0065..006FH	reserved	
0070H	Bit 6..0 = RealTimeClock/CMOS-RAM Address Register Bit 7 = Non Maskable Interrupt (NMI) Mask (write only)	
0071H	RealTimeClock/CMOS-RAM Data Register	
0072..007FH	reserved	
0080..0091H	DMA Page Registers / reserved	
0092H	Port 92h System Control Register	
0093..009FH	reserved	
00A0..00A1H	Slave Interrupt Controller	
00A2..00BFH	reserved	
00C0..00DFH	DMA Controller 2	
00E0..010FH	reserved	
0110..016FH	reserved	
0170..0177H	Secondary IDE Channel	
0178..01EFH	reserved	
01F0..01F7H	Primary IDE Channel	
01F8..01FFH	reserved	
0200..026FH	not used	
0278..027FH	reserved for Parallel Port (LPT2) and Plug'n Play	
0280..02E7H	reserved	
02E8..02EFH	Serial Port (COM4)	
02F0..02F7H	reserved	
02F8..02FFH	Serial Port (COM2)	
0300..036FH	not used	
0370..0377H	reserved for external Secondary Floppy Controller	
0376..0377H	reserved for external Secondary IDE Channel	
0378..037FH	Parallel Port (LPT1)	

Address	Description	
0380..03AFH	reserved	
03B0..03BBH	VGA registers (MDA)	
03BC..03BFH	reserved for Parallel Port (LPT3)	
03C0..03CFH	VGA registers (EGA)	
03D0..03DFH	VGA registers (CGA)	
03E0..03E7H	reserved	
03E8..03EFH	Serial Port (COM3)	
03F0..03F7H	reserved for external Primary Floppy Controller	
03F6..03F7H	Primary IDE Channel	
03F8..03FFH	Serial Port (COM1)	
0400..042FH	reserved	
0430..04EFH	reserved	
0480..048FH	DMA High Page Registers / reserved	
0490..049FH	Instruction Counter Registers / reserved	
04A0..04CFH	reserved	
04D0..04D1H	IRQ Edge/Level Control	
04D2..04FFH	reserved	
0500..08FFH	reserved	
0900..0A77H	reserved	
0A78H	Plug'n Play configuration port	
0A79..0BFFH	reserved	
0C00..0CF7H	reserved	
0CF8..0CFFH	PCI configuration registers	
0D00..0FFFH	reserved	
1000..3FFFH	reserved	
4000.. 46E7H	reserved	
46E8H	reserved	
46E9..47FFH	reserved	
4800..6FFFH	reserved	
7000..7FFFH	not used	
8000..81FFH	reserved	
8200..821FH	SL8 system registers	
8220..83FFH	reserved for Syslogic IPC add-on boards	
8400..BFFFH	reserved	
C000..FFFFH	reserved for PCI devices (VGA, Ethernet, USB, SATA)	

Tab. 5   I/O Address Space Layout

The processor module on the SL8 board offers a JTAG interface for factory operations on the internal header P11. These pins **must not** be connected by the user.

Pin Number	Signal	Remarks
1	TCK (do not connect)	
2	TDO (do not connect)	
3	TDI (do not connect)	
4	TMS (do not connect)	
5	TRST (do not connect)	
6	GND (do not connect)	

Tab. 6   Factory Programming Header P11 (1x6 pin)

The programmable logic device on the SL8 board is factory programmed using some pins of the internal header P12. These pins **must not** be connected by the user.

Pin Number	Signal	Remarks
1	TCK (do not connect)	
2	TDO (do not connect)	
3	TMS (do not connect)	
4	TDI (do not connect)	

Tab. 7   Factory Programming Header P12 (1x4 pin)

The power management controller on the SL8 board is factory programmed using the internal header P17. This header **must not** be connected by the user.

Pin Number	Signal	Remarks
1	VPP/MCLR# (do not connect)	PICkit3 pin 1
2	VCC (do not connect)	PICkit3 pin 2
3	GND (do not connect)	PICkit3 pin 3
4	PGD (ICSPDAT, do not connect)	PICkit3 pin 4
5	PGC (ICSPCLK, do not connect)	PICkit3 pin 5
6	PGM LVP (SCL, do not connect)	PICkit3 pin 6
7	-- (SDA, do not connect)	--

Tab. 8   Factory Programming Header P17 (1x7 pin)

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3.3. Peripheral Devices

3.3.1. DVI Interface

The DVI-D signals are available on the High Density DVI-D connector P5 for direct connection of DVI-D Single Link compatible monitors. The controller uses the standard VGA register interface. All configuration is done by software (BIOS, VGA-BIOS, OS driver).

Device Connection

Pin Number	Signal	Remarks
1	DATA#2	TMDS Link 1 Digital Red
2	DATA2	TMDS Link 1 Digital Red
3	Shield 2/4	connected to Ground
4	DATA#4	TMDS Link 2 not supported
5	DATA4	TMDS Link 2 not supported
6	DDC_CLK	DDC Clock
7	DDC_DATA	DDC Data
8	VSYNC	Analog VGA not supported
9	DATA#1	TMDS Link 1 Digital Green
10	DATA1	TMDS Link 1 Digital Green
11	Shield 1/3	Connected to Ground
12	DATA#3	TMDS Link 2 not supported
13	DATA3	TMDS Link 2 not supported
14	VCC5	+5Vdc standby power for monitor
15	GND	Ground
16	HPDET	Hot Plug Detect
17	DATA#0	TMDS Link 1 Digital Blue
18	DATA0	TMDS Link 1 Digital Blue
19	Shield 0/5	connected to Ground
20	DATA#5	TMDS Link 2 not supported
21	DATA5	TMDS Link 2 not supported
22	Shield CLK	connected to Ground
23	CLK	TMDS Clock
24	CLK#	TMDS Clock
C1	VGA_RED	Analog VGA not supported
C2	VGA_GREEN	Analog VGA not supported
C3	VGA_BLUE	Analog VGA not supported
C4	HSYNC	Analog VGA not supported
C5	VGA_GND	Analog VGA not supported

Tab. 9   DVI-D connector P5 (DSUB15HD)

Important Note

Maximum cable length for DVI-D connection is dependent on pixel clock frequency (about 5 m for 1920x1200 resolution).
Use high quality shielded DVI-D cables (with twisted diff pair wires for TMDS signals) for maximum EMI protection.

3.3.2. LVDS Display-Interface (optional)

The LVDS display interface is an optional interface for direct connection of an external TFT display. It supports 3.3V 8-bit Single and Dual Link LVDS TFT panels on connector P32. Direct inverter connection is provided through P31 if power requirement is not to high.

Note that special BIOS-Settings are required for operation of the LVDS display interface. Contact Syslogic technical support for details.

Device Connection (LVDS-Panel)

Mating connector type: Hirose DF13-40DS-1.25C, Crimp contact DF13-3032SCF.

Pin Number	Signal	Pin Number	Remarks
1	VCC_LCD (3.3Vdc)	2	VCC_LCD (3.3Vdc)
3	GND	4	GND
5	LVDS_A0-	6	LVDS_A0+
7	GND	8	LVDS_A1-
9	LVDS_A1+	10	GND
11	LVDS_A2-	12	LVDS_A2+
13	GND	14	LVDS_ACLK0-
15	LVDS_ACLK0+	16	GND
17	LVDS_A3-	18	LVDS_A3+
19	FPMODE (Switch S5 bit 2) Mode control (off=1k pullup to 3.3V / on=ground)	20	FPHMODE (Switch S5 bit 3) Mode control (off=1k pullup to 3.3V / on=ground)
21	GND	22	GND
23	LVDS_B0-	24	LVDS_B0+
25	GND	26	LVDS_B1-
27	LVDS_B1+	28	GND
29	LVDS_B2-	30	LVDS_B2+
31	GND	32	LVDS_BCLK0-
33	LVDS_BCLK0+	34	GND
35	LVDS_B3-	36	LVDS_B3+
37	GND	38	VCC_LCD5 (5Vdc)
39	VCC_LCD5 (5Vdc)	40	VCC_LCD5 (5Vdc)

Tab. 10 LVDS connector P32 (Hirose DF13A-40DP-1.25V)

Important Note
Do not draw more than 1.0 Ampere from VCC_LCD (max. 0.5 Ampere per pin).
This interface is intended for case internal use only.

◇ **syslogic**

Device Connection (Backlight)

Mating connector type: Housing Molex 51021-0600, Crimp contact Molex 50058-8100.

Wiring: AWG26.

Pin Number	Signal	Remarks
1	VCC_INV	Inverter Power 12V
2	VCC_INV	Inverter Power 12V
3	GND	Ground
4	GND	Ground
5	EN	Inverter enable
6	LCD Brightness (0..5V)	Brightness Control

Tab. 11 Backlight connector P31 (Molex 53398-0871)

Important Note

Do not draw more than 1.0 Ampere from VCC_INV (max. 0.5 Ampere per pin).

Check inverter board datasheet for polarity of brightness control and other requirements.

This interface is intended for case internal use only.

Device Configuration (Display and Backlight Control)

Display configuration (FBHMODE, FPMODE) and backlight control (Analog/PWM) must be set using switch S5 and S1. Please check display and backlight datasheet for required settings.

Switch S5	FPH MODE	FP MODE	Backlight Control	Remarks
0	1	1	Analog 0-2.5V	
1	1	1	Analog 0-5V	
2	1	1	PWM 0-3.3V	
3	1	1	PWM 0-5V	
4	1	0	Analog 0-2.5V	
5	1	0	Analog 0-5V	
6	1	0	PWM 0-3.3V	
7	1	0	PWM 0-5V	
8	0	1	Analog 0-2.5V	
9	0	1	Analog 0-5V	
A	0	1	PWM 0-3.3V	
B	0	1	PWM 0-5V	
C	0	0	Analog 0-2.5V	
D	0	0	Analog 0-5V	
E	0	0	PWM 0-3.3V	
F	0	0	PWM 0-5V	

Tab. 12 LVDS Configuration Options

For S1 settings see Tab. 3.

Important Note

Switch S5 must be set correctly **before** applying power.

False settings may damage display and/or backlight.

3.3.3. High Definition Audio

INTEL High Definition Audio interface is integrated in the ATOM E38xx processor.

Device Connection

Mating connector type: IDC Receptable FCI 20021444-00010T4LF.

Wiring: Ribbon cable AWG30.

Pin Number	Signal	Remarks
1	SDATA_IN	
2	SDATA_OUT	
3	RST#	Reset
4	SYNC	
5	GND	
6	BITCLK	
7	GND	
8	SPKR	
9	+V5S	5V supply *
10	+V3.3S	3.3V supply *

Tab. 13 HDAudio interface connector P47

Important Note

This interface is intended for case internal use only.

3.3.4. Buzzer Interface / Buzzer (optional)

A standard buzzer interface is available on internal connector P3 for connection of a PC buzzer like TDK SD1209T5-A1 or similar type. The buzzer drive signal is generated by the standard PC timer 1. It is buffered by an open collector NPN transistor and protected by a free-wheeling diode against inductive load spikes.

Optionally the buzzer interface can be replaced by a buzzer directly on board.

Device Connection

Mating connector type: Housing Molex 51021-0200, Crimp contact Molex 50058-8100.
Wiring: AWG26.

Pin Number	Signal	Remarks
1	BUZ+ (5V)	not fused
2	BUZ- (buzzer drive signal)	100mA max

Tab. 14 Buzzer interface connector P3

Important Note

This interface is intended for case internal use only.

⬢ **syslogic**

3.3.5. CFast-Interface / SATA (optional)

The SL8 features an SATA generation 2 hostcontroller having assigned the base address and IRQ at boot time by the PCI-BIOS.

Channel 0 of the SATA controller serves the CFast socket P8. The CFast card behaves like a standard SATA disk. Channel 1 serves the standard SATA connector P81.

Tested CFast cards are:
- Cactus Technologies KC-series

Device Connection (CFast)

.

Pin Number	Signal	Pin Number	Signal
S1	SGND	PC1	CDI
S2	RxP	PC2	GND
S3	RxN	PC3	nc
S4	SGND	PC4	nc
S5	TxN	PC5	nc
S6	TxP	PC6	nc
S7	SGND	PC7	GND
		PC8	LED1
		PC9	LED2
		PC10	IO1
		PC11	IO2
		PC12	IO3
		PC13	PWR
		PC14	PWR
		PC15	PGND
		PC16	PGND
		PC17	CDO

Tab. 15 CFast Connector P8 (SATA Channel 0)

Important Note

Do not insert or remove the CFast card when power supply is on. This interface does not support hot-plugging.

Device Connection (SATA Data)

.

Pin Number	Signal	Remarks
1	GND	
2	TX+	
3	TX-	
4	GND	
5	RX-	
6	RX+	
7	GND	
8	G1	
9	G2	

Tab. 16 SATA Data Connector P81 (SATA Channel 1)

Device Connection (SATA Power)

Mating connector type: Housing Molex Micro-Fit 3.0 order number 43645-0200, Crimp contact Molex 43030 series.

Pin Number	Signal	Remarks
1	VCC	+5V (not fused)
2	GND	

Tab. 17 SATA Power Connector P82 (SATA Channel 1)

⬡ **syslogic**

3.3.6. Serial Ports

Up to four serial ports are available with standard RS232 signals. Two of them are available on standard DSUB-9 connectors on the front (COM1, COM2), the others are available on internal headers (COM3, COM4).

The serial ports have fixed base addresses of 3F8H for COM1, 2F8H for COM2, 3E8H for COM3 and 2E8H for COM4.

COM1 uses hardware interrupt 4, COM2 uses hardware interrupt 3, COM3 uses hardware interrupt 10 and COM4 uses hardware interrupt 5. Interrupt configuration may be changed in CMOS setup SIO configuration.

Device Connection RS232

The Serial Port COM1 is available on DSUB-9 connector P14.
The Serial Port COM2 is available on DSUB-9 connector P15.
The Serial Port COM3 is available on the internal header P43.
The Serial Port COM4 is available on the internal header P44.

Pin Number	Signal	Pin Number	Signal
1	DCD*	6	DSR*
2	RXD	7	RTS*
3	TXD	8	CTS*
4	DTR*	9	RI*
5	GND		

Tab. 18 Serial Ports COM1-2 on DSUB-9 male P14, P15 (9 pin)

Pin Number	Signal	Pin Number	Signal
1	DCD*	2	DSR*
3	RXD	4	RTS*
5	TXD	6	CTS*
7	DTR*	8	RI*
9	GND	10	+5V (not fused)

Tab. 19 Serial Ports COM3-4 internal Headers P43-44 (2x5 pin)

Configuration Options RS485 (COM2 only in selected products)

Switch	Configuration	Remarks
S17: 1	OFF = COM2 full duplex RS485 (RS422) ON = COM2 half duplex RS485	requires BIOS CMOS parameter COM2 "Auto Direction Control" set to "ON, high active"

Tab. 20 RS485 Configuration Options

Device Connection RS485 (COM2 only in selected products)

The Serial Port COM2/RS485 is available on connector P15.

120 Ohm termination resistors must be connected externally!

Pin Number	Signal	Pin Number	Signal
1	no connection	6	no connection
2	RX-	7	RX+
3	TX-	8	TX+
4	no connection	9	no connection
5	RGND		

Tab. 21 Full duplex RS485 ports COM2 on DSUB-9 male P15 (9 pin)

Pin Number	Signal	Pin Number	Signal
1	no connection	6	no connection
2	no connection	7	no connection
3	DATA-	8	DATA+
4	no connection	9	no connection
5	RGND		

Tab. 22   Half duplex RS485 ports COM2 on DSUB-9 male P15 (9 pin)

Important Note

In RS485 mode the transmit driver is enabled while sending only. To get full RS422 compatibility in full duplex mode the transmit driver must be forced to stay always enabled. For this the BIOS CMOS parameter COM2 "Auto Direction Control" must be set to "OFF" and the user application must manually set the COM2 RTS# signal to high level (deactivated). Note that some serial port tools and os drivers may overwrite the RTS# state later which must be prevented.

3.3.7. Keyboard Interface (optional)

The keyboard signals are available on connector P4 for connection of PS/2 style keyboards. The controller uses hardware interrupt 1 for the keyboard. It may be enabled/disabled in CMOS setup SIO configuration.

Device Connection

Mating connector type: Housing Molex 51021-0400, Crimp contact Molex 50058-8100.
Wiring: AWG26.

Pin Number	Signal	Remarks
1	+5V (not fused)	
2	KBDATA	
3	KBCLK	
4	GND	

Tab. 23 PS/2 Keyboard connector P4

Important Note

Maximum cable length allowed for keyboard connection is 3 m.
Use shielded cables for maximum EMI protection.

⬢ **syslogic**

3.3.8. USB Interface

The SL8 features an OHCI/EHCI and a XHCI compatible USB host controller having assigned the base address and IRQ at boot time by the PCI-BIOS. All ports support USB 2.0 devices and port 1 supports USB 3.0 devices with Superspeed.

Device Connection

The USB interface uses two standard A type double USB connector on the front for USB ports 1/2 and 3/4. Ports 5 and 6 are located on two internal 4 pin connectors.

Mating connector type for P22, P23: Housing Harwin DataMate M80-8880405, Crimp contacts included (M80-0130005). Recommended wire type: BS3G210 type A, PTFE insulated, 24-28AWG, max insulation diameter 1.10mm. Twist D+/D- wires.

P20 bottom Pin Number	USB port 1 Signal	P20 top Pin Number	USB port 2 Signal
1	VBUS	1	VBUS
2	D-	2	D-
3	D+	3	D+
4	GND	4	GND

Tab. 24 USB1/2 Interface Connector P20 (Dual Type A)

P20 bottom Pin Number	USB port 3 Signal	P20 top Pin Number	USB port 4 Signal
1	VBUS	1	VBUS
2	D-	2	D-
3	D+	3	D+
4	GND	4	GND

Tab. 25 USB3/4 Interface Connector P21 (Dual Type A)

Pin Number	Signal	Remarks
1	D+	
2	D-	
3	VBUS	
4	GND	

Tab. 26 USB5/6 Interface Connector P22 and P23 (2x2pin)

> **Important Note**
>
> Maximum cable length allowed for USB connection is 3 m. If longer cables are used, special overvoltage and filtering elements have to be installed to comply with the requirements of EMI/RFI "CE"-certification. Only use high quality industrial USB devices with sufficient EMI compatibility.
>
> Use shielded cables for maximum EMI protection.
>
> Drawing excessively power might disturb operation.

3.3.9. CAN Interfaces

Up to two CAN 2.0b interfaces using standalone SJA1000-similar PCIe CAN controllers. The controllers are compatible with PEAK-System PCIe CAN controllers and include a license to use the PEAK-System drivers.

CAN i/o base address and interrupt enumerated by PCIe BIOS.

CAN2 requires a special driver board. Please contact factory for availability

Configuration Options CAN (only available in selected products)

Switch	Configuration	Remarks
S17: 2	OFF = 2 CAN channels enabled ON = 1 CAN channel enabled	2nd channel requires special driver board

Tab. 27 CAN Configuration Options

Device Connection CAN (only available in selected products)

The CAN interface is available on connector P15.

120 Ohm termination resistors must be connected externally!

Pin Number	Signal	Pin Number	Signal
1	no connection	6	no connection
2	CAN Low	7	CAN High
3	CAN Ground	8	no connection
4	no connection	9	no connection
5	no connection		

Tab. 28 CAN port CAN1 on DSUB-9 male P15 (9 pin)

Pin Number	Signal	Remarks
1	+5V (not fused)	
2	RX CAN2	3.3V LVCMOS
3	TX CAN2	3.3V LVCMOS
4	GND	

Tab. 29 CAN port CAN2 on connector P70

3.3.10. Ethernet LAN Interface

The SL8 features up to two PCI Ethernet controller having assigned the base address and IRQ at boot time by the BIOS. The Ethernet interface drives two LED's (yellow and green) integrated into the RJ45 connector for status information. The meaning of the LED activity is programmable (normally set by the low level driver).

LAN1 and LAN2 feature Intel I210 Ethernet controllers supporting 10/100/1000Mb/s. Both interfaces support Auto Negotiation and Auto MDIX functions. Check manufacturer's datasheets for detailed information.

No configuration options are available for the Ethernet device.

Device Connection

The Ethernet interfaces use the standard RJ45 Gigabit connector P18 and P19 on the front for 100Ω shielded or unshielded Twisted Pair cabling.

Pin Number	Signal	Remarks
1	MD0+	
2	MD0-	
3	MD1+	
4	MD2+	
5	MD2-	
6	MD1-	
7	MD3+	
8	MD3-	

Tab. 30 Ethernet Twisted Pair Interface Connector P18 and P19 (RJ45)

3.3.11. Wireless interface

According to the product configuration several wireless interfaces are available on ANT1 – ANT3 on the backside of the device.

Device Connection

Standard SMA connector with 50Ω cable impedance

3.3.12. I2C Interface

The SL8 features one I2C interface on an internal connector on the PC/104 bus expansion rows F/E (see paragraph 3.3.18 for details). The interface is integrated into the processor module (see processor module datasheet for details). The signals are non-buffered 3.3V LVCMOS interfaces with integrated pullups.
Consult processor module datasheet for programming details.

Device Connection I2C

The first I2C interface uses connector P46. Mating connector type: Housing Molex 51021-0400, Crimp contact Molex 50058-8100. Wiring: AWG26.

Pin Number	Signal	Remarks
1	VCC (3.3V)	not fused!
2	SDA	3.3V LVCMOS with integrated pullup
3	SCL	3.3V LVCMOS with integrated pullup
4	GND	

Tab. 31 I2C Interface Connector P46

Important Note

This interface is intended for case internal use only.

3.3.13. Watchdog

The watchdog timer is configurable for 100 ms or 1 s base (default) timeout. Longer timeouts may be achieved by programming the Watchdog Configuration Register.
Once timed out, it may activate the SL8 hardware reset or the processors NMI line depending on software configuration.

Configuration Options

Switch	Configuration	Remarks

| S1 | even positions '0', '2', '4', '6', '8' = 1 s | see Tab. 3. |
| | odd positions '1', '3', '5', '7' = 100 ms | see Tab. 3. |

Tab. 32 Watchdog Configuration Options

3.3.14. Power supply

The processor and its peripherals are powered by a non-isolated, integrated power supply which generates all the necessary voltages.

The power must be connected using the following mating connector:

Weidmueller BCZ 3.81/04/180F SN SW (Ordercode 1792970000).

 The mating connector can be ordered directly at your local Weidmueller distributor .

Pin Number	Signal	Remarks
1	+24VDC_AUX	Auxiliary power supply
2	Power Fail/Remote on/off	Power fail input
3	+24VDC	+9V..+30V DC
4	GND	

Tab. 33 Power supply connector

For normal operation the external power supply has to be connected to the pins 3 (+24VDC) and 4 (GND) of the connector.

Pin 1 (+24VDC_AUX) may be used as a standby supply for the optional GoldCap RTC backup.

Pin 2 is used as an input for either a power fail or remote on/off signal.

3.3.15. Power supervision

The power management control unit (PCU) can be operated in two modes: power fail mode or remote on/off mode. The following two chapters describe their functionality in detail.

Switch	Configuration	Remarks
S12	position '0' = test mode (powerfail active)	check chapter
	position '1' = internal pulldown (remote on/off mode)	3.3.16/3.3.17
	position '2' = internal pullup (power fail mode)	
	position '3' to 'F' = reserved (do not use)	

Tab. 34 Power fail input configuration

Switch	Configuration	Remarks
S14	position '0' = bypass mode (for power fail mode)	check chapter
	position '1' to 'F' = remote on/off mode	3.3.16/3.3.17

Tab. 35 Power fail mode configuration

3.3.16. Power Fail

In power fail mode the microcontroller monitors the external power fail signal. The state of power fail signal can be access through the status register, I/O 8200h.

Application example
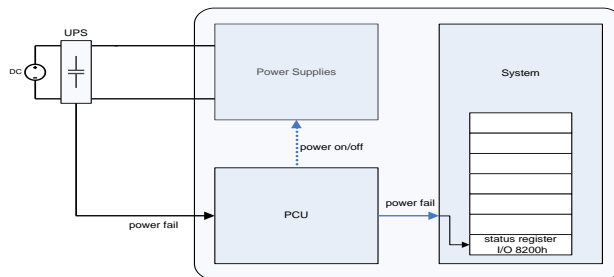
Fig. 6   Typical power fail application

The application has to poll the power fail flag and call different functions according to the state of the flag.
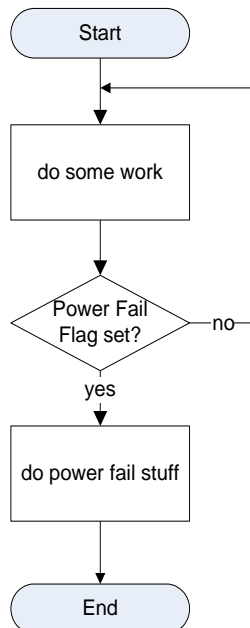
Fig. 7   Typical power fail flow

3.3.17. Remote On/Off

With the remote on/off function the system can be switched on and off through an external control signal. When active the internal software goes from the run state into the shutdown state. After a predefined timeout the PCU switches the main power supply off. The timeout can be configured through S14. Mode 6-9 are controlled by a 250ms Impulse of the external control signal. Mode 8 and 9 have the feature to do a hard power off when the Impulse is longer than 5 seconds.

Config switch S14 position	$t_{debounce\_on}$ On debouncing (setup)	$t_{debounce\_off}$ Off debouncing (hold)	$t_{startup}$ Hold time until switch off signal is routed to processor, if system is still booting	t_{hard_off} Timeout until switch off signal is generated from processor (after that hard off)
0	-	-	-	-
1	2 s	60 s	5 s	60 s
2	2 s	60 s	60 s	300 s
3	2 s	60 s	60 s	120 s
4	1 s	5 s	5 s	60 s
5	5 s	5 s	60 s	60 s
6	0 s	0 s	60 s	60 s
7	0 s	0 s	60 s	60 s
8	0 s	0 s	60 s	60 s
9	0 s	0 s	60 s	0 s
5 – F	n/a	n/a	n/a	n/a

Tab. 36 PCU timing configuration through S14

When switch S14 is in position 0 the PCU is in bypass mode.
Please check the separate documentation and sample code for details about the programming of the power management control unit.

Application example
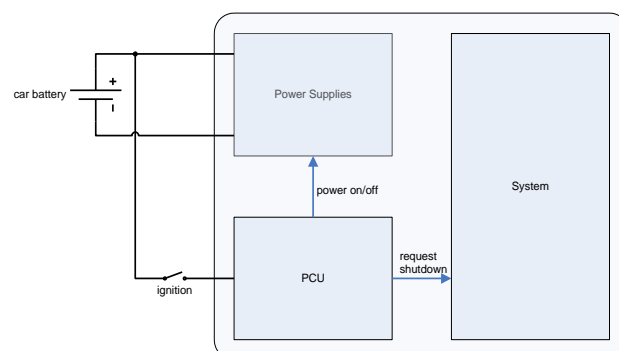
Fig. 8   Application example: CAR PC

Startup sequence
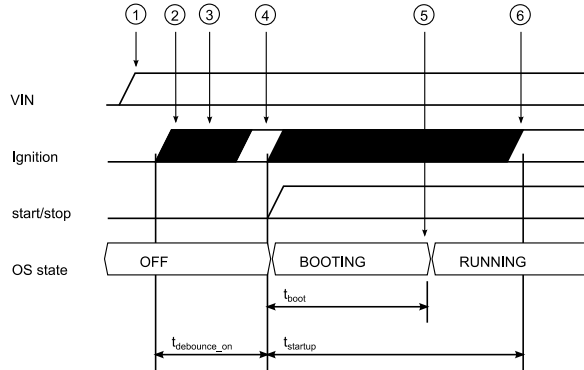
Notes:

1) VIN supply must be present

2) Ignition on starts debouncing sequence

3) glitches/bounces are ignored during $t_{debounce\_on}$

4) if ignition signal is stable after $t_{debounce\_on}$, supply is switched on and the system starts

5) during $t_{startup}$, ignition switch is ignored
Note: system might have finished booting well in advance before startup phase is over

6) after $t_{startup}$, the power management circuit resumes tracking of the ignition switch signal

Fig. 9   Startup timing diagram

Forced shutdown sequence
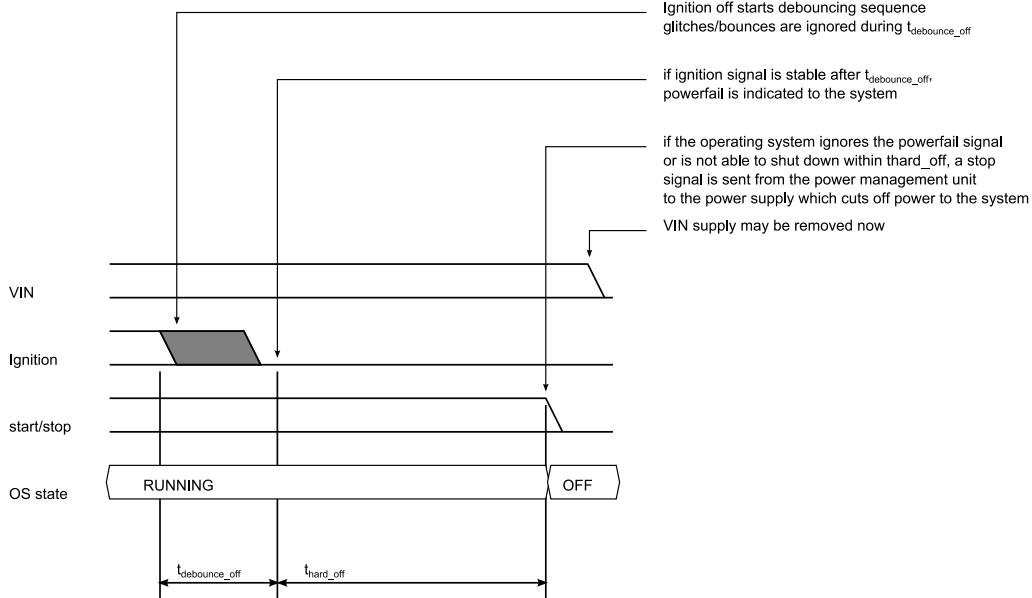
Ignition off starts debouncing sequence glitches/bounces are ignored during $t_{debounce\_off}$

if ignition signal is stable after $t_{debounce\_off}$, powerfail is indicated to the system

if the operating system ignores the powerfail signal or is not able to shut down within thard_off, a stop signal is sent from the power management unit to the power supply which cuts off power to the system

VIN supply may be removed now

Fig. 10   Shutdown timing diagram

Important Notes

The operating system must support the remote on/off function.

3.3.18. Expansion Bus Interface

The internal expansion bus interface of the S8 allows expansion with a range of I/O and communications boards. The bus connector pinout is shown in Tab. 38. See paragraph 7.1 for electrical specification.

Pin		Signal Name	Direction	Pin		Signal Name	Direction
A1	⊗	SATA_RX_P	input	B1	⊗	SATA_TX_P	output
A2	⊗	SATA_RX_N	input	B2	⊗	SATA_TX_N	output
A3	⊗	reserved		B3	⊗	USB_OC#	
A4	⊗	I2C_DAT	bidirectional	B4	⊗	USB_DP	bidirectional
A5	⊗	I2C_CLK	output	B5	⊗	USB_DN	bidirectional
A6	⊗	reserved		B6	⊗	USB_PWRON	
A7	⊗	PCIE_RX_P	input	B7	⊗	PCIE_TX_P	output
A8	⊗	PCIE_RX_N	innput	B8	⊗	PCIE_TX_N	output
A9	⊗	reserved		B9	⊗	reserved	
A10	⊗	PCIE_WAKE#	input	B10	⊗	PCIE_CLK_P	output
A11	⊗	PCIE_RST#	output	B11	⊗	PCIE_CLK_N	output
A12	⊗	reserved		B12	⊗	reserved	
A13	⊗	SMB_DAT	bidirectional	B13	⊗	LPC_RST#	output
A14	⊗	SMB_CLK	output	B14	⊗	LPC_CLK	output
A15	⊗	SMB_ALRT#	input	B15	⊗	LPC_FRAME#	output
A16	⊗	LPC_AD1	bidirectional	B16	⊗	LPC_AD0	bidirectional
A17	⊗	LPC_AD3	bidirectional	B17	⊗	LPC_AD2	bidirectional
A18	⊗	SERIRQ	input	B18	⊗	LPC_LDRQ	input
A19	⊗	SUS_S5#	output	B19	⊗	SUS_S3#	output
A20	⊗	+5V	power, always on	B20	⊗	+1.5V	power, always on
A21	⊗	+5V	power, always on	B21	⊗	+1.5V	power, always on
A22	⊗	+5V	power, always on	B22	⊗	+3.3V	power, always on
A23	⊗	+5V	power, always on	B23	⊗	+3.3V	power, always on
A24	⊗	+5V	power, always on	B24	⊗	+3.3V	power, always on
A25	⊗	+5V	power, always on	B25	⊗	+3.3V	power, always on

Tab. 37 Expansion Bus Connector P51

3.3.19. PC/104 Bus Interface

The internal PC/104 bus interface of the SL8 allows expansion with a wide range of I/O and communications boards. The bus interface is described in the IEEE 996 and 996.1 standards documentation. The bus connector pinout is shown in Tab. 38. See paragraph 7.1 for electrical specification.

Pin		Signal Name	Pin		Signal Name	Pin		Signal Name	Pin		Signal Name
						A1	⊗	IOCHCK#	B1	⊗	GND
						A2	⊗	SD7	B2	⊗	RESETDRV
F1	⊗	GND	E1	⊗	GND	A3	⊗	SD6	B3	⊗	+5V
F2	⊗	I2C_CLK	E2	⊗	+5V	A4	⊗	SD5	B4	⊗	IRQ9
F3	⊗	I2C_DAT	E3	⊗	I2C_ALRT#	A5	⊗	SD4	B5	⊗	-5V (optional)
F4	⊗	Vbatt	E4	⊗	STOP#	A6	⊗	SD3	B6	⊗	DRQ2
F5	⊗	+12V (optional)	E5	⊗	+12V (optional)	A7	⊗	SD2	B7	⊗	-12V (optional)
F6	⊗	GND (optional)	E6	⊗	GND (optional)	A8	⊗	SD1	B8	⊗	0WS#
D0	⊗	GND	C0	⊗	GND	A9	⊗	SD0	B9	⊗	+12V (optional)
D1	⊗	MEMCS16#	C1	⊗	SBHE#	A10	⊗	IOCHRDY	B10	⊗	(KEY)
D2	⊗	IOCS16#	C2	⊗	LA23	A11	⊗	AEN	B11	⊗	SMEMW#
D3	⊗	IRQ10	C3	⊗	LA22	A12	⊗	SA19	B12	⊗	SMEMR#
D4	⊗	IRQ11	C4	⊗	LA21	A13	⊗	SA18	B13	⊗	IOW#
D5	⊗	IRQ12	C5	⊗	LA20	A14	⊗	SA17	B14	⊗	IOR#
D6	⊗	IRQ15	C6	⊗	LA19	A15	⊗	SA16	B15	⊗	DACK3#
D7	⊗	IRQ14	C7	⊗	LA18	A16	⊗	SA15	B16	⊗	DRQ3
D8	⊗	DACK0#	C8	⊗	LA17	A17	⊗	SA14	B17	⊗	DACK1#
D9	⊗	DRQ0	C9	⊗	MEMR#	A18	⊗	SA13	B18	⊗	DRQ1
D10	⊗	DACK5#	C10	⊗	MEMW#	A19	⊗	SA12	B19	⊗	REFRESH#
D11	⊗	DRQ5	C11	⊗	SD8	A20	⊗	SA11	B20	⊗	SYSCLK
D12	⊗	DACK6#	C12	⊗	SD9	A21	⊗	SA10	B21	⊗	IRQ7
D13	⊗	DRQ6	C13	⊗	SD10	A22	⊗	SA9	B22	⊗	IRQ6
D14	⊗	DACK7#	C14	⊗	SD11	A23	⊗	SA8	B23	⊗	IRQ5
D15	⊗	DRQ7	C15	⊗	SD12	A24	⊗	SA7	B24	⊗	IRQ4
D16	⊗	+5V	C16	⊗	SD13	A25	⊗	SA6	B25	⊗	IRQ3
D17	⊗	MASTER#	C17	⊗	SD14	A26	⊗	SA5	B26	⊗	DACK2#
D18	⊗	GND	C18	⊗	SD15	A27	⊗	SA4	B27	⊗	TC
D19	⊗	GND	C19	⊗	(KEY)	A28	⊗	SA3	B28	⊗	BALE
D20	⊗	reserved	C20	⊗	reserved	A29	⊗	SA2	B29	⊗	+5V
D21	⊗	reserved	C21	⊗	reserved	A30	⊗	SA1	B30	⊗	OSC
						A31	⊗	SA0	B31	⊗	GND
						A32	⊗	GND	B32	⊗	GND

Tab. 38 PC/104 Bus Connectors PA/PB, PC/PD

The SL8 board is not fully IEEE 996.1 (PC/104) compliant. The following restrictions and differences to the IEEE 996.1 specification apply:
- connector is compatible but the monting holes are not
- The interrupt lines are pulled up with 8k2 resistors to Vcc (EISA specification) instead of 2k2 (IEEE 996)
- only 8 bit I/O transfers are supported
- 16 bit I/O and memory and 8 bit memory transfers are not supported
- DMA transfers are not supported
- MASTER# transfers are not supported

The following restrictions apply to the additional bus signals:
- I2C_ALRT# is not supported
- +12V, -12V and -5V are not supported

Important Note

Do not connect bus drivers/receivers with integrated bushold circuit to the PC/104 signals. This may disturb proper operation of the SL8 board or add-on boards.

3.3.20. Frontside Status LEDs

The four colored LEDs on the front side show the following states:

LED	Signal	Remarks
Red up	STOP signal	programming see Control register in chapter 4
Green down	Board ready	programming see Setup register in chapter 4
Green up	Aux LED	programming see Setup register in chapter 4
Yellow down	Disk activity	SATA/CFast only

4 Programming Information

4.1. Overview

The programming of the SL8 board is done with standard memory and I/O read and write operations. Most configuration options are handled by the BIOS. For detailed information refer to the NETIPC firmware documentation and other related documents as listed in paragraph 1.3. Please contact Syslogic technical support if you need special BIOS configuration.

4.2. Interrupt, Memory and I/O Resources

4.2.1. Interrupt Resources

The following table shows the usage of the interrupt resources. Interrupts marked 'shared' are shared between an onboard device and an PC/104 bus interrupt line. These interrupts should only be used for multiple interrupt sources, if all interrupt routines are able to process shared interrupts. Interrupts marked 'free' are not used by onboard devices if they are not assigned to a PCI device in the BIOS configuration. Interrupts for use on the PC/104 bus must be configured as 'reserved' in CMOS setup legacy interrupt configuration and must not be used by SIO peripherals (check SIO configuration in CMOS setup).

Interrupt	Interrupt Source	Remarks
Master		
IRQ0	Timer Channel 0	
IRQ1	PS/2-Controller (Keyboard)	SIO, check CMOS setup
IRQ2	Slave Interrupt Controller Cascading	
IRQ3	COM2	SIO, check CMOS setup
IRQ4	COM1	SIO, check CMOS setup
IRQ5	available for PCI or COM4	SIO, check CMOS setup
IRQ6	available for PCI or PC/104 Bus IRQ6	check CMOS setup
IRQ7	available for PCI or LPT1	SIO, check CMOS setup
Slave		
IRQ8	Real Time Clock	
IRQ9	ACPI/PCI	do not connect
IRQ10	available for PCI or COM3	SIO, check CMOS setup
IRQ11	available for PCI or PC/104 Bus IRQ11	check CMOS setup
IRQ12	available for PCI or PS/2-Controller	SIO, check CMOS setup
IRQ13	Floating Point Unit	
IRQ14	Primary IDE/SATA Channel in legacy mode	do not connect
IRQ15	available for PCI or PC/104 Bus IRQ15	check CMOS setup
Special		
NMI	Watchdog and PC/104 Bus Error Interrupt IOCHCK*	shared

Tab. 39 Interrupt Usage

4.2.2. Memory Resources

The general memory layout is shown in paragraph 3.2.1. The configuration of the memory layout is done by programming processors internal configuration registers and board configuration registers (see paragraph 4.2.3). This is done completely by the BIOS on system startup and must not be changed during operation. For operating systems requiring memory configuration (e.g. Windows CE) the memory layout shown in paragraph 3.2.1 must be considered.

4.2.3. I/O Resources

This paragraph describes only the SL8 system register and support functions not directly related to a specific peripheral device. The general I/O layout is shown in paragraph 3.2.2. Peripheral devices are discussed in paragraph 0. Note that the Socket Memory related registers are programmed by the BIOS on system startup and must not be changed during operation.

Address	Device / Register	Remarks
8200H	Status Register	
8201H	Control Register	Reset state = 05H
8202H	Function ID Register	
8203H	Watchdog Configuration Register	Reset state = 80H
8204H	Option ID Register	
8205H	Setup Register	Reset state = 00H
8206H	Revision ID Register	
8207H	Socket Memory Configuration Register	not supported
8208H	Socket Memory Window Mapping Register	not supported
8209H	Socket Memory Window Base Address Register	not supported
820AH	Boot Mode Input Register	
820BH	I2C Register for Temp Sensor	
820CH	Configuration Switch Input register	
820DH	PWM-Register for LCD Inverter Brightness Control	Reset state = FFH
820E..821FH	reserved	do not access

Tab. 40 SL8 System Registers

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Status Register 8200h

D7	D6	D5	D4	D3	D2	D1	D0	Access
OVRTMP#	LOBAT#	1	WDG#	ERRFLG#	ATTFLG#	IOCHCK#	PF#	Read
reserved								Write
1111'1111 (0xFF)								Reset

Description:

OVRTMP# Temperature Sensor Status Flag

Read	Write
0 = programmed temp. limit reached 1 = temperature ok (below limit)	

LOBAT# Battery Status Flag

Read	Write
0 = Battery voltage low 1 = Battery voltage ok	

WDG# Watchdog Status Flag

Read	Write
0 = Watchdog has timed out 1 = Watchdog running or disabled Reset by issuing a hardware reset (see register 8204hex)	

ERRFLG# Error Status Flag (for polled applications)

Read	Write
not used, returns 1	

ATTFLG# Attention Status Flag (for polled applications)

Read	Write
not used, returns 1	

IOCHCK# IOCHCK# Status (PC/104 bus)

Read	Write
0 = IOCHCK# active 1 = IOCHCK# inactive	

PF# Power Fail Status Flag (for polled applications)

Read	Write
0 = Power Fail active 1 = Power Fail inactive	

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Control Register 8201h

D7	D6	D5	D4	D3	D2	D1	D0	Access
TRIG#	WDTRIG	WDNMI	STOP	TRGSRC	FREEZE	ERREN#	ATTEN#	Read
TRIG#	WDTRIG	WDNMI	STOP	TRGSRC	FREEZE	ERREN#	ATTEN#	Write
0000'0101 (05h)								Reset

Description:

TRIG#   Bus Trigger (currently not supported)

Read	Write
readback of written value	

WDTRIG   Watchdog Trigger

Read	Write
readback of written value	Any state change triggers the watchdog.

WDNMI   Watchdog NMI Configuration

Read	Write
0 = Watchdog activates hardware reset 1 = Watchdog timeout activates Non Maskable Interrupt (NMI)	0 = Watchdog activates hardware reset 1 = Watchdog timeout activates Non Maskable Interrupt (NMI)

STOP   NETSBC Stop# Signal State

Read	Write
0 = STOP# inactive (high), red LED off 1 = STOP# active (low), red LED on	0 = STOP# inactive (high), red LED off 1 = STOP# active (low), red LED on

TRGSRC   Trigger source selection

Read	Write
not used, returns 0	

FREEZE   Freeze bit

Read	Write
not used, returns 1	

ERREN#   Error Interrupt Enable (PC/104 bus IOCHCK# routed to NMI)

Read	Write
always 0 = Error Interrupt on NMI always enabled	

ATTEN#   Attention Interrupt Enable

Read	Write
not used, returns 1	

The STOP# signal is intended for control of add-on boards. It is available on the PC/104 bus connector extension PE.

STOP# is intended as signal to force an add-on board function to a specified state. For example with the digital I/O board IPC/DIO32 the STOP# signal is used to either reset or freeze the state of the digital outputs depending on setup of the DIO32 board as long as the STOP# signal is active (low).
The STOP# signal also directly drives the red LED on the front (STOP# low = LED on).
Upon startup STOP# is active (LED on) until the BIOS has initialized the main peripherals, it is set inactive (LED off) before booting the operating system. STOP# is also active (LED on) while operating in Bootloader mode.

Function ID Register 8202h

D7	D6	D5	D4	D3	D2	D1	D0	Access
FID[7:0] Function ID								Read
reserved, always write 0								Write
same as Read value								Reset

Description:

FID   Function ID

Read	Write
51h = general IPC processor board	reserved, always write 0

Watchdog Configuration Register 8203h

D7	D6	D5	D4	D3	D2	D1	D0	Access
WDLOCK	0	0	0	WDTOUT[3:0] Watchdog Timeout Selection				Read
WDLOCK	reserved	reserved	reserved	WDTOUT[3:0] Watchdog Timeout Selection				Write
1000'0000 (80h)								Reset

Description:

WDLOCK   Watchdog Lock Flag (prevents disabling running Watchdog)

Read	Write
0 = Inactive, not locked	0 = do not lock
1 = Active, locked	1 = lock WDEN

WDTOUT   Watchdog Timeout Selection

Read	Write
0 = 1s if S1=even, 100ms if S1=odd	0 = 1s if S1=even, 100ms if S1=odd
1 = 4s	1 = 4s
2 = 8s	2 = 8s
3 = 16s	3 = 16s
4 = 32s	4 = 32s
5 = 64s	5 = 64s
6 = 128s	6 = 128s
7 = 256s	7 = 256s

reserved   Reserved, always write 0

Note

Watchdog timeout selection values > 0 are independent of switch S1 setting.

Option ID Register 8204h

D7	D6	D5	D4	D3	D2	D1	D0	Access
OID[7:0] Option ID								Read
reserved, always write 0								Write
same as Read value								Reset

Description:

OID   Option ID

Read	Write
D0h = ML8/SL8	A5h = Writing data A5h invokes a complete hardware reset (also clearing the Watchdog timeout status bit) 5Ah = Writing data 5Ah invokes a complete power off or power reset (also clearing the Watchdog timeout status bit), system restarts depending on configuration of power management controller.

Setup Register 8205h

D7	D6	D5	D4	D3	D2	D1	D0	Access
READY	WDEN	AUX	0	0	USBEN2	USBEN1	USBEN0	Read
READY	WDEN	AUX	0	0	USBEN2	USBEN1	USBEN0	Write
0000'0111 (07h)								Reset

Description:

READY   Ready bit, green LED

Read	Write
0 = Inactive, green LED off	0 = Deactivate green LED
1 = Active, green LED on	1 = Activate green LED

WDEN   Watchdog enable

Read	Write
0 = Watchdog disabled	0 = Disable watchdog
1 = Watchdog enabled (running)	1 = Enable watchdog

AUX   Auxiliary LED, green LED

Read	Write
0 = Inactive, green AUX LED off	0 = Deactivate green AUX LED
1 = Active, green AUX LED on	1 = Activate green AUX LED

USBEN2   USB4/5 Power enable

Read	Write
0 = USB5/6 power off	0 = disable USB5/6 power
1 = USB5/6 power on	1 = enable USB5/6 power

USBEN1   USB2/3 Power enable

Read	Write
0 = USB3/4 power off	0 = disable USB3/4 power
1 = USB3/4 power on	1 = enable USB3/4 power

USBEN0   USB0/1 Power enable

Read	Write
0 = USB1/2 power off	0 = disable USB1/2 power
1 = USB1/2 power on	1 = enable USB1/2 power

The READY signal directly drives the green LED on the front (READY high = LED on).
Upon startup READY is inactive (LED off) until the BIOS has initialized the main peripherals,
it is set active (LED on) before booting the operating system.
Always read back the current state before programming this setup register for enabling the
watchdog!

Important Note

Be careful when disabling USB power by setting USBENx=0 since this will disable any all devices connected to the two related USB ports. Always use a program sequence which automatically reenables USB power some seconds later.

Revision ID Register 8206h

D7	D6	D5	D4	D3	D2	D1	D0	Access
RID[7:0] Revision ID								Read
reserved, always write 0								Write
same as Read value								Reset

Description:

RID   Logic Design Revision ID

Read	Write
see Product Revision History	

reserved   Reserved, always write 0

Socket Memory Configuration Register 8207h

D7	D6	D5	D4	D3	D2	D1	D0	Access
0	0	0	0	0	0	0	0	Read
reserved								Write
0000'0000 (0x00)								Reset

Description:

Reserved   reserved

Read	Write
0	

Reserved   reserved, do not write

Socket Memory Window Mapping Register 8208h

D7	D6	D5	D4	D3	D2	D1	D0	Access
0	0	0	0	0	0	0	0	Read
reserved								Write
0000'0000 (0x00)								Reset

Description:

Reserved   reserved

Read	Write
0	

Reserved   reserved, do not write

Socket Memory Window Base Address Register 8209h

D7	D6	D5	D4	D3	D2	D1	D0	Access
0	0	0	0	0	0	0	0	Read
reserved								Write
0000'0000 (0x00)								Reset

Description:

Reserved   reserved

Read	Write
0	

Reserved   reserved, do not write

Status Register 820Ah

D7	D6	D5	D4	D3	D2	D1	D0	Access
0	0	0	0	0	0	BM1	BM0	Read
reserved								Write
0000'0011 (0x03)								Reset

Description:

BM1..0   Boot Mode Inputs

Read	Write
0 = reserved	
1 = reserved	
2 = boot from backup BIOS	
3 = normal Operating Mode	

Reserved   reserved, do not write

I2C Register 820Bh for temperature sensor control

D7	D6	D5	D4	D3	D2	D1	D0	Access
SCLO	SDAO	SCL	SDA	1	1	1	1	Read
SCLO	SDAO	Reserved, always write 1						Write
FFh								Reset

Description:

SCLO   Clock Port Output State

Read	Write
0 = Pin state = low 1 = Pin state = high	0 = Output latch state = low 1 = Output latch state = high (open collector)

SDAO   Data Port Output Port Latch State

Read	Write
0 = Pin state = low 1 = Pin state = high	0 = Output latch state = low 1 = Output latch state = high (open collector)

SCL   Clock Port Pin State

Read	Write
0 = Pin state = low 1 = Pin state = high	

SDA   Data Port Pin State

Read	Write
0 = Pin state = low 1 = Pin state = high	

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Configuration Switch Input Register 820Ch

D7	D6	D5	D4	D3	D2	D1	D0	Access
0	0	0	0	S1-D3	S1-D2	S1-D1	S1-D0	Read
reserved								Write
xxxx'xxxx (0xXX)								Reset

Description:

D3-0   Configuration Switch S1 Inputs

Read	Write
S1 state (0-F)	

D7-4   Configuration Switch Inputs

Read	Write
0 (reserved)	

Reserved   reserved, do not write

PWM Register 820Dh for LCD Inverter Brightness Control

D7	D6	D5	D4	D3	D2	D1	D0	Access
PWM preset D[7..0]								Read
PWM preset D[7..0]								Write
FFh								Reset

Description:

D[7..0]   PWM Preset Register

Read	Write
D[7..0] = Preset Value	D[7..0] = Preset Value

The PWM value, may be translated to a voltage depending on setting of configuration switch S5. Value 0 corresponds to voltage level 0, value FFh corresponds to maximum voltage level (2.5V or 5V). Signal may be inverted by setting of switch S1 (see Tab. 3).
Please check inverter datasheet for translation of voltage level to brightness.

4.3. Peripheral Devices

4.3.1. DVI/LCD-Interface

The DVI/LCD interface uses the standard PC/AT VGA register set. For detailed programming information please refer to the IBM PC/AT Technical Reference or similar documentation. Low level programming is handled by the VESA compatible VGA-BIOS.
For custom LCD BIOS requirements please contact Syslogic technical support.
For detailed programming information please refer to the Intel Atom E38xx technical reference or similar documentation. Legacy support and low level programming is handled by the BIOS and standard OS drivers.

4.3.2. SATA/CFast-Interface

For detailed programming information please refer to the Intel Atom E38xx technical reference or similar documentation. Legacy support and low level programming is handled by the BIOS and standard OS drivers.

4.3.3. Serial Ports

The Serial Port interfaces use the standard PC/AT register set. The Serial Port controller is compatible with the standard 16C550A UART with 16 byte receive and transmit fifos. For detailed programming information please refer to the IBM PC/AT Technical Reference, the SMSC SCH3114 datasheet or similar documentation. Legacy support and low level programming is handled by the BIOS and standard OS drivers.
For transmitter control in RS485/RS422 mode see paragraph 3.3.6 (selected variants only).

4.3.4. Keyboard Interface

The Keyboard interface uses the standard PC/AT register set. The keyboard controller is compatible with the standard Intel 8042 device with integrated keyboard host controller firmware. For detailed programming information please refer to the IBM PC/AT and PS/2 Technical Reference, the SMSC SCH3114 datasheet or similar documentation. Legacy support and low level programming is handled by the BIOS and standard OS drivers.

4.3.5. Ethernet Interface

The Ethernet interfaces use the Intel I210IT Ethernet Controller. For detailed programming information and drivers check www.intel.com .

4.3.6. USB Interface

The USB interfaces use the standard OHCI/EHCI/XHCI register set. Legacy support and low level programming is handled by the BIOS and standard OS drivers.

4.3.7. CAN Interface

The CAN interfaces are are compatible with PEAK-System PCIe CAN controllers and include a license to use the PEAK-System drivers. For detailed programming information and drivers check PCAN-miniPCIe download section on www.peak-system.com .

4.3.8. Temperature Sensor

The Temperature Sensor is built up using an LM75 compatible temperature sensor programmable through an I2C interface. The I2C interface programming is done through the I2C Register of the SL8. For detailed programming information please refer to the National Semiconductor LM75 datasheet or similar documentation.

Poweron default setting for OVERTMP* is 80°C chip temperature.

4.3.9. Watchdog

The watchdog is disabled by default on poweron and must be enabled by the application program.

Before enabling the watchdog by setting the WDEN bit in the SL8 Setup Register, the watchdog action (RESET or NMI) must be programmed in the SL8 Control Register (bit WDNMI) and the timeout value must be configured using switch S1 and/or the SL8 Watchdog Configuration Register.

If RESET activation is selected, the watchdog generates a hardware reset if it is not triggered within the configured timeout window by writing the WDTRIG bit in the SL8 Control Register. The application must check the WDG* bit in the SL8 Status Register upon startup to identify the Watchdog as the source of the reset, and it must issue a hardware reset (by writing the value 0a5h to the SL8 Option ID Register) to clear the WDG* flag. Otherwise the system resets again as soon as the Watchdog is started.

If NMI activation is selected, the watchdog generates a Non Maskable Interrupt to the processor if it is not triggered within the configured timeout window by writing the WDTRIG bit in the SL8 Control Register. Note that enabling the NMI input of the processor also requires setting bit 7 of I/O port 70h (NMI mask) and clearing bit 3 of I/O port 61h (Port B IOCHK# enable). The NMI routine must check the WDG* bit in the SL8 Status Register to identify the watchdog as the source of the NMI, and it must issue a hardware reset (by writing the value 0a5h to the SL8 Option ID Register) to clear the WDG* flag. Otherwise the NMI routine is entered again as soon as the watchdog is started.

Sample code showing the initialization and triggering of the watchdog is available for RESET and NMI mode in the free IPC/IOCOMSW-1A package.

Note

The NMI mask bit (bit 7 of I/O port 70h) is write only. Typically it is enabled by the BIOS and should not be disabled by application software.

4.3.10. Expansion Bus Interface

For detailed description of expansion bus add-on board programming please consult the add-on boards documentation.

4.3.11. PC/104 Bus Interface

For detailed description of PC/104 add-on board programming please consult PC/104 and ISA bus standard documentation and related PC/AT architecture literature as well as the add-on boards documentation.

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5 Installation and cabling

5.1. Introduction

Installation and cabling of the IPC/SL8 system has to be done with great care; the correct cabling is essential for high operational reliability and the correct grounding is necessary for protection. To meet the requirements of "CE"-certification all cables have to be shielded. The enclosure has to be connected to ground via the DIN-rail or mounting kit.

Important note

Before applying power to the SL8 system, the main board must be configured correctly.

Important notes

To meet the requirements of EMI/RFI "CE"-certification, correct mounting, installation and cabling of the SL8 system according to these guidelines is absolutely necessary.

5.2. Powering the SL8 System

The "logic supply voltage", i.e. the power driving the electronic circuits (CPU and base board) is internally generated from the 12/24VDC power supply input. Remember that the power supply is non-isolated. For an isolated version please contact the manufacturer.

The power supply has to be connected according to paragraph 3.3.14. Maximum allowed cable length between ac/dc power supply and system power input is 30 m. If the cable is longer than 30 m or routed outside the building, special overvoltage and filtering elements have to be installed to comply with the requirements of EMI/RFI "CE"-certification. Use AWG18/0.75mm^2 wires at minimum to comply with the safety requirements and follow the connector manufacturers instruction guide.

When selecting the external power supply the maximum power dissipation of the system has to be considered.

Important notes

Please make sure that the input voltage does not exceed the recommended operating range otherwise the electronics board could get damaged and correct operation cannot be guaranteed.

Use an overload protected power supply to prevent damage in case of a short inside the system.

The ac/dc power supply must fulfill the requirements for EMI/RFI "CE"-certification.

> **Warning**
>
> The device requires a current limited power supply. Use a 4AT fuse or a power supply that does not exceed 4A max.

5.3. Cabling the interfaces

Use appropriate cabling for all interfaces. Shielded cabling is required to meet the EMI/EMC limits.

5.4. Grounding

In some cases it is recommended to connect the shields of the cables to chassis potential at the entry point into the housing cabinet as shown in Fig. 11. If the cables enter a hermetically closed cabinet, use special 360 degree metal clamps (EMI/RFI protected types which contact to the cable shield).

> **Important notes**
>
> Grounding of the cables shields using "pig-tail wires" are not recommended because of their high impedance at high frequencies. It is better to clamp the shields onto a grounded copper rail.
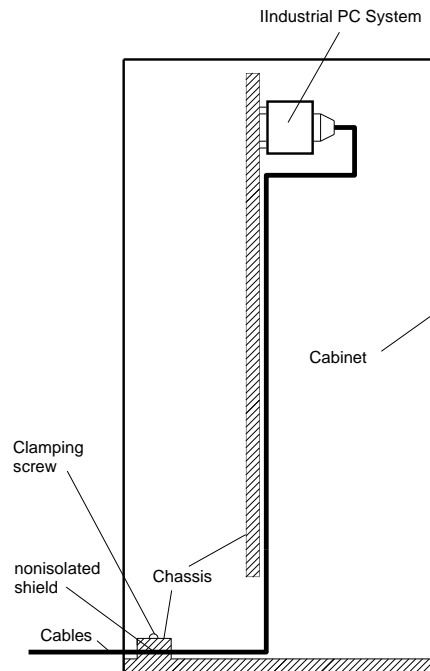
Fig. 11 Additional grounding of the cable shields at the entry point of a cabinet.

5.5. Cabling of communication links

If the communication ports are unisolated ports, cable shields have to be connected to chassis potential on both sides of the interconnection cable. If the cable is very long, a thick copper wire (10 mm^2) for potential adjustment is highly recommended.

Fig. 12 shows an non isolated system with common chassis ground.

Some of the communication ports are galvanically isolated ports. In such cases the shield of the interconnection cable must be wired to chassis potential only on one side of the cable. Fig. 13 shows an isolated system with independent grounds.

Important notes

Grounding of cable shields using "pig-tails wires" are not recommended because of their high impedance at high frequencies. It is recommended to clamp the shields onto a grounded copper-rail.
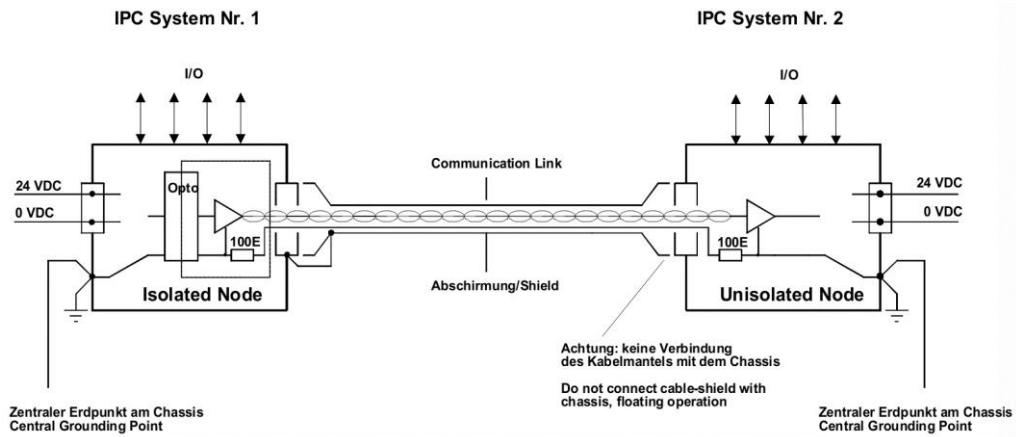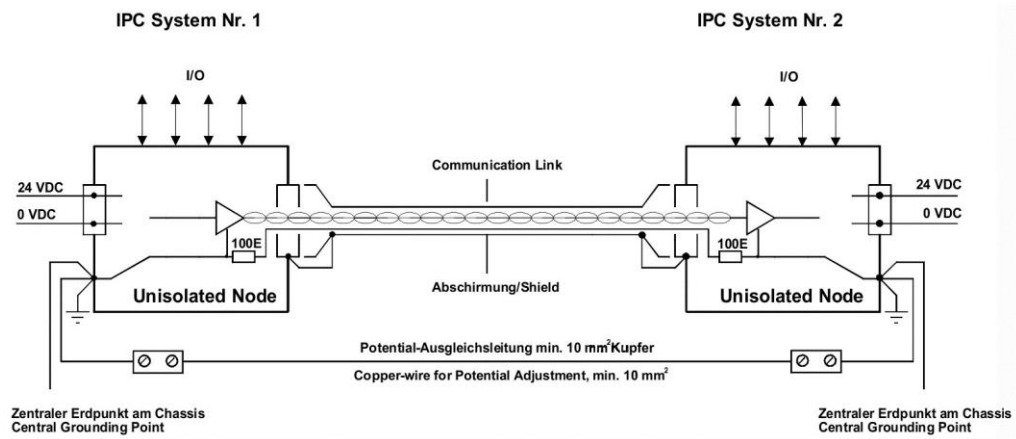

Fig. 12   Isolated communication link

Fig. 13   Non isolated communication link with common chassis potential

6 Service

6.1. Replaceable Parts

This SL8 system contains the following replaceable parts:

- CFast flash card
- Litium battery
- Main fuse

To replace the flash card power off the system and remove the service cover. After having unlocked the clip, the flash card may be removed. When inserting a new flash card be sure that it is fully compliant with the CFast standard. Syslogic highly recommends CFast flash cards specified for industrial use by the card manufacturer. Check temperature range and durability to comply with your requirements.

To replace the battery power off the system and remove the service cover. Pull out the battery carefully.

Replacement battery must be one of the following types:

- Renata CR2450N (3V, 540mAh)
- Renata CR2477N (3V, 950mAh)

Because the self-discharge of all Lithium Batteries increases rapidly at high temperatures the battery life time decreases by a great amount. To prevent battery leakage scheduled service/replacement is recommended. Please contact the battery manufacturer for further details and calculation assistance for battery life time calculation.

The main fuse protects the system against destruction in case of high energy distortions on the power line. For replacement, the system must be opened in a ESD protected environment. Only an entitled instructed person is allowed for this operation. Replacement fuse type is Littlefuse 452004.MRL (4A slow-blow).

Safety warnings and installation guidelines must be followed according to paragraphs 1.6, 1.8 and 5.

Fig. 14   Service parts replacement

7 Technical Data

7.1. Electrical Data

> **Important Note**
>
> Do not operate the SL8 system outside of the recommended operating conditions. Otherwise lifetime and performance will degrade. Operating the board outside of the absolute maximum ratings may damage the hardware.

Absolute Maximum Ratings (over free-air temperature range)

Parameter	Symbol	min	nom	max	Unit
power supply voltage	Vcc	-0.5		30	Vdc
isolation logic to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		100	500		Vrms
isolation LAN/RJ45 to logic (AC, 60s, 500m a.s.l., Ta=25°C)		1500			Vrms
isolation LAN/RJ45 to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation CAN to logic (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation CAN to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
creepage distances:					
logic to chassis and PCB boarder		1.0			mm
logic to mounting holes		1.0			mm
operating free-air temperature (Ambient)	Ta	-40		70	°C
storage temperature range[1]	Tst	-40		85	°C

Tab. 41 General Absolute Maximum Ratings

[1]Due to the large effect of self-discharge at high temperature of the Lithium Battery it is recommended to store the device at around +25°C.

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Recommended Operating Conditions

Parameter	Symbol	min	nom	max	
power supply voltage	Vcc	9.0	12/24	30	Vdc
battery backup voltage (Io=100µA)	Vbatt	2.7	3.0	3.3	Vdc
SATA connector (P82) power load (+5V)	Isata			500	mA
PS/2 connector (P4) power load (+5V)	Ips2			50	mA

operating free-air temperature range
  IPC/SL8G13 50% CPU load, high GPU load [1]
  IPC/SL8H19 50% CPU load, low GPU load [1]
	Ta	-40		70	°C

operating free-air temperature range IPC/SL8H19 50% CPU load, high GPU load [1]	Ta	-40		65	°C
(1) this parameter is highly dependent on mounting, air flow and GPU load; with the Intel SpeedStep technology the processor automatically reduces the internal cpu clock down to 500MHz when the critical thermal trip points are reached to prevent damage.					

Tab. 42 General Recommended Operating Conditions

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Electrical Characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	typ	max	Unit
general parameters					
full load power dissipation (worst case, no external loads, IPC/SL8H19-A101E)	Pmax		15	18	W
full load power dissipation (worst case, no external loads, IPC/SL8G13-A101E)	Pmax		10	13	W
power supply current (Vcc=24V, no external loads, IPC/SL8H19-A101E)	Icc		0.3		A
power supply current (Vcc=12V, no external loads, IPC/SL8H19-A101E)	Icc		0.5		A
power fail / remote on/off					
inactive state	PFhigh	2.3		Vp	V
active state	PFlow	-0.5		2.3	V
RTC backup battery					
Vbatt loading (Vcc=off)	Ibat(off)		4	5	uA
Vbatt loading (Vcc=on)	Ibat(on)		2	4	uA
Backup time with new CR2450N battery (Ta=25°C)	t(rtcbup)	6	7		years
Backup time with new CR2450N battery (Ta=50°C)	t(rtcbup)	3	3.5		years
Backup time with new CR2477N battery (Ta=25°C)	t(rtcbup)	8	9		years
Backup time with new CR2477N battery (Ta=50°C)	t(rtcbup)	3.5	4		years
LOWBAT* trip point		2.35	2.5	2.65	V
VRT trip point (RTC Valid RAM and Time Flag)			1.3		V
LCD backlight control					
LCD inverter enable control disable state	Il<4mA	0		0.4	V
LCD inverter enable control enable state	Ih<4mA	2.4		3.3	V
LCD inverter brightness control	I=10mA	0		5	V
USB Overcurrent Limit					
USB on internal connector P23	Ilimit		2.8		A
all other USB connectors	Ilimit		1.5		A
CAN Isolation					
Isolation resistance CAN signals to case/shield	R(iso)		1		MOhm

Tab. 43 General Electrical Characteristics

Important Note
Battery backup time is highly dependent on temperature and on/off cycling profile.

Switching Characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	nom	max	
processor characteristics					
processor clock (IPC/SL8G13-xxx)	fcpu		1.33		GHz
processor clock (IPC/SL8H19-xxx)	fcpu		1.91		GHz
communication interface characteristics					
UART base clock	fuart		1.8459		MHz
COM1/2/3/4 baud rate				115.2	kbaud
timer/clock characteristics					
Watchdog timeout (short period)	Tw	70	100	140	ms
Watchdog timeout (long period)	Tw	0.7	1	1.3	s
Timer base clock	ftimer		1.19318		MHz
Timer base clock accuracy				+/-100	ppm
Timer base clock aging				+/-5	ppm/year
Real Time Clock base clock	frtc		32.768		kHz
Real Time Clock accuracy (25°C)				+/-20	ppm
Real Time Clock temperature coefficient				-0.04	ppm/(°C)²
Real Time Clock aging				+/-3	ppm/year
LCD inverter brightness PWM base clock	fpwm		16		kHz

Tab. 44 General Switching Characteristics

7.2. EMI/EMC Data

The SL8 system fulfills the following standards:

Emission: EN55032 / CISPR 32 Class A
EN55022 / CISPR 22 Class A
EN55011 / CISPR 11 Class A
Immunity: EN55024 / CISPR 24 Class A
EN61000-6-2 / EN61000-6-1

Important Note
The SL8 system is a class A system for industrial applications. It is not indented for use in residential or home applications.
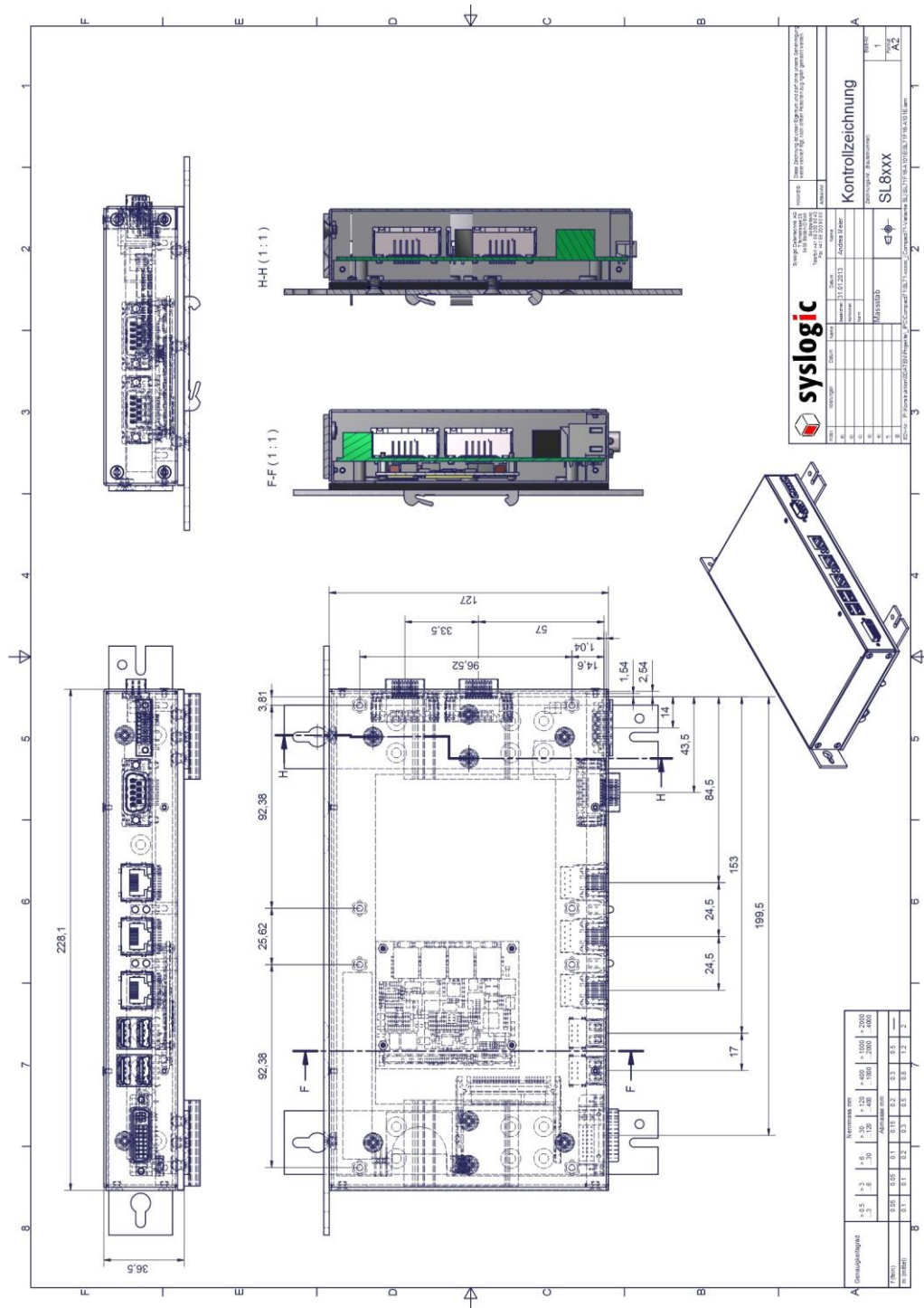
7.3. Mechanical Data

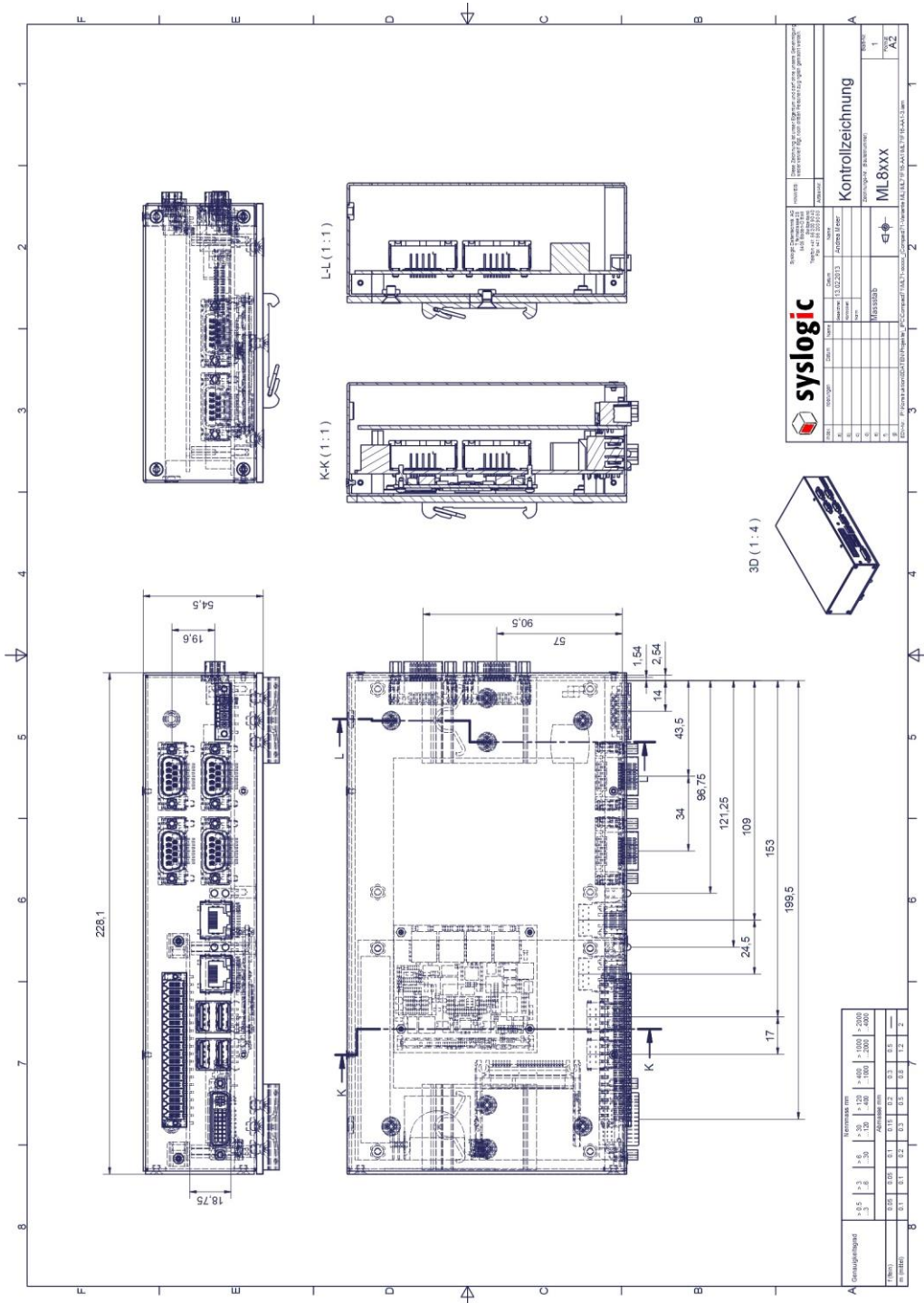Fig. 15   Mechanical Outline Enclosure SL
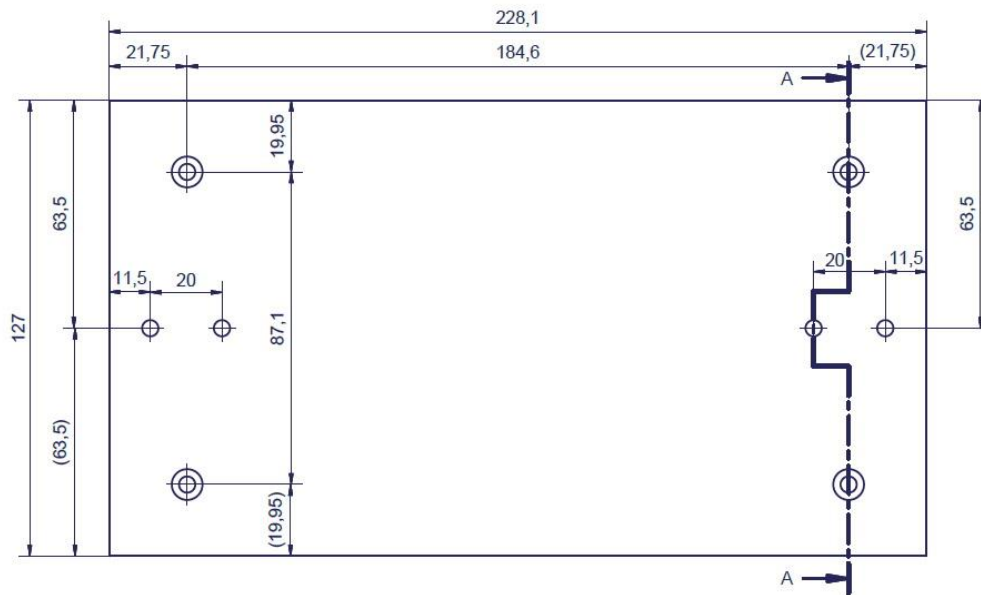
Fig. 16   Mechanical Outline Enclosure ML

Fig. 17   Mounting Plate

8 Firmware

8.1. Software Structure

The x86 CPU board based PC/104 system is based on the following software structure:

BIOS (Basic Input/Output System)

- Power On Self Test (POST)
- Initialization of standard peripheral devices
- Boot procedure for the Operating System
  Note : Refer to the BIOS documentation for detailed information

OS (Operating System)

- Initialization of additional peripheral devices
- Start procedure for the Application Programs
  Note : Refer to the OS documentation for detailed information

Application Programs

- Initialization of SL8 system, communications and external devices
- Start procedure for the Control Tasks
  Note : Refer to the Application Programs documentation for detailed information

8.2. Firmware Functions

The SL8 board is setup with BIOS firmware. Some standard PC/AT peripheral devices (e.g. DVI, Keyboard/Mouse, Serial Ports, SATA interface) are directly supported by the BIOS, BIOS extensions and Operating Systems. Some peripheral devices (e.g. Ethernet) are directly supported by standard communication software (e.g. TCP/IP stacks, TCP packet drivers) others need special programming according to the freely available sample software IPC/IOCOMSW-1A (e.g. Watchdog). Please refer to the appropriate documentation for detailed information.

8.3. Application Programming Interface (API)

The SL8 system does not contain any special API beside the installed BIOS. Refer to the BIOS and Operating System documentation for API specifications.

9 Product Revision History

9.1. Hardware

This paragraph lists the different hardware revisions of the SL8 systems delivered beginning with the first production lot. Note that prototyping boards are not included and must be returned to factory for upgrade or replacement. All information listed in this document relies on definitive state hardware. Therefore this information may be incompatible with the prototyping board hardware.

Board Identification (see product label)	Product Revision	Revision ID Register	Remarks
IPC/ xL8xxx-AxxxE #1	1	01H	Original Release
IPC/ xL8xxx-AxxxE #1	1	03H	support for high speed expansion board added
IPC/ xL8xxx-AxxxE #1	1	04H	support for Apollo Lake variants added

Tab. 45 Hardware Revision State

9.2. Firmware

This paragraph lists the different firmware versions of the SL8 systems delivered beginning with the first production lot. Note that prototyping boards are not included and must be returned to factory for upgrade or replacement. All information listed in this document relies on definitive state hardware. Therefore this information may be incompatible with the prototyping board hardware.

Board Identification (see product label)	BIOS Version	Build Date	Remarks
IPC/ xL8Gxx-AxxxE #xx	S8D1R001	06.02.2015	Original Release 1.0
IPC/ xL8Hxx-AxxxE #xx	S8D2R001	06.02.2015	Original Release 1.0
IPC/ xL8Gxx-AxxxE #xx	S8D1R011	27.06.2016	Release 2.0
IPC/ xL8Hxx-AxxxE #xx	S8D2R011	27.06.2016	Release 2.0
IPC/ xL8Gxx-AxxxE #xx	D1R011B	27.06.2016	3.1, default CMOS settings for USB adjusted
IPC/ xL8Hxx-AxxxE #xx	D2R011B	27.06.2016	3.1, Default CMOS settings for USB adjusted

Tab. 46 Firmware Revision State

9.3. Erratas

This paragraph lists some important erratas of the current SL8 boards to enable workarounds in user software. Additional erratas might be present but a workaround already implemented in the BIOS. It is important therefore that neither the application software nor the operating systems reprograms the processor chipset's configuration registers.

Note that prototype board erratas (boards with revision #0) are not listed here. Contact Syslogic technical support for prototype board information.

Additional erratas of the processor chipset can be found at:

https://www.intel.com/content/dam/www/public/us/en/documents/specification-updates/atom-e3800-family-spec-update.pdf

IOCHCK#/Watchdog-NMI bug (not working)	
Problem	When Watchdog is configured to activate an NMI or signal IOCHCK# on PC/104 interface is activated, the NMI service routine is not called.
Implication	IOCHCK#/Watchdog-NMI not usable.
Workaround	none.
Correction	This bug might be a BIOS problem and will be corrected in a future BIOS release.
SDCard Interface bug (not working with some SDCard types)	
Problem	The Intel processor chipset contains several issues in SD and SDIO Hostcontroller which can disturb normal operation of the SDCard interface.
Implication	Some SDCard types will not work reliable.
Workaround	Some of the issues have already been solved by a BIOS workaround, some are dependent on OS drivers and some are not fixable. Check with Syslogic for a list of working SDCard types. Some SDCards work if the BIOS setting Advanced > SCC Configuration > SCC eMMC Support is set to eMMC AUTO MODE. Additionally, SDR25 Support for SD Card should be set to enabled. Changes only become active when the BIOS is exited with Save Changes and Exit.
Correction	Some of the issues might be solved by new BIOS and/or OS driver releases, but some are not fixable.

Important Note

This document always covers the latest product revision listed in Tab 45, 46.

Please contact the manufacturers technical support for upgrade options.

⬨ **syslogic**

10 Manufacturer Information

10.1. Contact

Our distributors and system integrators will gladly give you any information about our products and their use. If you want to contact the manufacturer directly, please send an email message containing a short description of your application and your request to the following address or use one of the information or technical support request forms on our internet homepage:

Syslogic Datentechnik AG, Switzerland

Web: http://www.syslogic.com

Email: info@syslogic.com

Technical support: support@syslogic.com

10.2. Warranty

Our products are covered by a world-wide manufacturer's warranty. The warranty period starts at the delivery time from our official distributor to the customer. The duration of the warranty period is specified in the respective product catalogs and the offers. All products carry a job number for identification. The manufacturing data and deliveries are registered in a high level Quality Management System.

The warranty covers material and manufacturing defects. All products must be returned via the official distributor to the factory for repair or replacement. The warranty expires immediately if the products are damaged of operation outside of the specified recommended operating conditions. The warranty also expires if the date code or job number listed on the product is altered or rendered unintelligible. The warranty does not include damage due to errors in firmware or software delivered with the products.

10.3. RMA Service

Syslogic offers a Return Material Authorization process to simplify handling of devices that needs to be returned to the manufacturer. Please follow the instructions on our web page: https://www.syslogic.com to get best service.